EM78P302N

8-BIT Microcontroller

Product Specification

DOC. VERSION 1.2

ELAN MICROELECTRONICS CORP.

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ELAN MICROELECTRONICS CORPORATION

Headquarters:
No. 12, Innovation 1st Road
Hsinchu Science Park
Hsinchu, TAIWAN 30076
Tel: +886 3 563-9977
Fax: +886 3 563-9966
webmaster@emc.com.tw
http://www.emc.com.tw

Hong Kong:
Elan (HK) Microelectronics Corporation, Ltd.
Flat A, 19F., World Tech Centre
95 How Ming Street, Kwun Tong
Kowloon, HONG KONG
Tel: +852 2723-3376
Fax: +852 2723-7780

USA :
Elan Information Technology Group (U.S.A.)
PO Box 601
Cupertino, CA 95015
U.S.A.
Tel: +1 408 366-8225
Fax: +1 408 366-8225

Shenzhen:
Elan Microelectronics Shenzhen, Ltd.
8A Floor, Microprofit Building
Gaoxin South Road 6
Shenzhen Hi-Tech Industrial Park
South Area, Shenzhen
CHINA 518057
Tel: +86 755 2601-0565
Fax: +86 755 2601-0500
elan-sz@elanic.com.cn

Shanghai:
Elan Microelectronics Shanghai, Ltd.
6F, Ke Yuan Building
No. 5 Bibo Road
Zhangjiang Hi-Tech Park
Shanghai, CHINA 201203
Tel: +86 21 5080-3866
Fax: +86 21 5080-0273
elan-sh@elanic.com.cn

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APPENDIX

Specification Revision History

Version	Revision Description	Date
0.9	Preliminary version	2015/06/05
1.0	Initial release version	2016/04/20
1.1	1. Modified User Application Note 2. Added usage of TCC function in Section 7.3	2016/06/16
1.2	1. Modified AD converter characteristics	2016/07/26

User Application Note

(Before using this chip, take a look at the following description note, it includes important messages.)

1. The value in the dead-time register must be less than the value in the duty cycle register, in order to prevent unexpected behavior on both of the PWM outputs.

2. The PWM output will not be set, if the duty cycle is “0”.

3. The internal TCC will stop running when in sleep mode. However, during AD conversion, when TCC is set to “SLEP” instruction, if the ADWE bit of the RE register is enabled, TCC will keep on running.

4. During ADC conversion, do not perform output instruction to maintain precision for all of the pins. In order to obtain accurate values, it is necessary to avoid any data transition on the I/O pins during AD conversion

5. The noise rejection function is turned off in the LXT2 and sleep mode.

6. Low Voltage Reset (LVR) is designed for unstable power situation. If the EM78P302N is targeted to operate at 8 MHz, the working voltage should be avoided to drop below 2.5V. The LVR does not work in this case when the working voltage is between 2.5V and POR level.

7. We strongly recommend that user has to place external pull-down or pull-high resistor (0Ω/1kΩ/10kΩ/100kΩ) on P55 no matter what the pin function is (except Crystal Mode). The purpose of this is to prevent P55 from floating.

8. The maximum of integral non-linearity (INL) in Analog-to-Digital converter (ADC) with internal reference voltage (2.0V/2.5V/3.0V/4.0V) is ±12 LSB.

9. You must reload TCC (R1) before reset TCC overflow interrupt flag.

1 General Description

The EM78P302N is an 8-bit microprocessor designed and developed with low-power and high-speed CMOS technology. The device has an on-chip 1.25K×13-bit Electrical One Time Programmable Read Only Memory (OTP-ROM). It provides a protection bit to prevent intrusion of user's OTP memory code. Three Code option bits are also available to meet user's requirements.

With enhanced OTP-ROM features, the EM78P302N provides a convenient way of developing and verifying user's programs. Moreover, this OTP device offers the advantages of easy and effective program updates, using development and programming tools. User can avail of the ELAN Writer to easily program his development code.

2 Features

- CPU configuration
  - 1.25k × 13 bits on-chip ROM
  - 80 × 8 bits on-chip registers (SRAM)
  - 8-level stacks for subroutine nesting
  - 3 programmable Level Voltage Reset (LVR) : 4.0V, 3.5V, 2.7V
  - Less than 1.5 mA at 5V / 4 MHz
  - Typically 15 μA, at 3V / 32 kHz
  - Typically 2 μA, during sleep mode
- I/O port configuration
  - 3 bidirectional I/O ports: P5, P6, P7
  - 12 I/O pins
  - Wake-up ports : P5, P70, P71
  - 8 programmable pull-down I/O pins
  - 10 programmable pull-high I/O pins
  - 2 programmable open-drain I/O pins
  - 8 high driver I/O pins
  - 8 high sink I/O pins
  - External interrupt : P60
- Operating voltage range:
  - 2.1V ~ 5.5V at 0°C ~ 70°C (commercial)
  - 2.3V ~ 5.5V at -40°C ~ 85°C (industrial)
- Operating frequency range (based on 2 clocks):
  - Crystal mode: DC ~ 16 MHz, 3.0V;
    DC ~ 8MHz, 2.5V; DC ~ 4 MHz, 2.1V
  - I RC mode
    Oscillation mode: 4 MHz, 16 MHz, 8 MHz, 1 MHz

Internal RC Frequency	Drift Rate			
	Temperature (-40°C~85°C)	Voltage (2.1V~5.5V)	Process	Total
4 MHz	±2%	±1%	±1%	±4%
16 MHz	±2%	±1%	±1%	±4%
8 MHz	±2%	±1%	±1%	±4%
1 MHz	±2%	±1%	±1%	±4%

- Fast set-up time requires only 0.8ms (VDD: 5V, Crystal: 4 MHz, C1/C2: 30pF) in HXT2 mode and 10μs in IRC mode (VDD: 5V, IRC: 4MHz)
- Peripheral configuration
  - 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
  - 8-bit multi-channel Analog-to-Digital Converter with 12-bit resolution in Vref mode
  - Two Pulse Width Modulation (PWM) with 8-bit resolution.
- Nine available interrupts
  - TCC overflow interrupt
  - Input-port status changed interrupt (wake up from sleep mode)
  - External interrupt
  - ADC completion interrupt
  - PWM period match interrupt
  - PWM duty match interrupt
- Special Features:
  - Programmable free running Watchdog Timer (4.5ms, 18ms)
  - Power saving Sleep mode
  - Selectable Oscillation mode
  - Power-on voltage detector available (1.9V ± 0.2V)
  - High EFT immunity (better performance at 4 MHz or below)
- Package Type:
  - 10-pin MSOP 118mil : EM78P302NMS10
  - 14-pin DIP 300mil : EM78P302ND14
  - 14-pin SOP 150mil : EM78P302NSO14

Note: *These are all Green products which do not contain hazardous substances.*

3 Applications

- Charger
- Control board of an air conditioner
- Electromagnetic-stove
- Washing machine
- Toaster
- Coffee pot

4 Pin Assignment (Package)

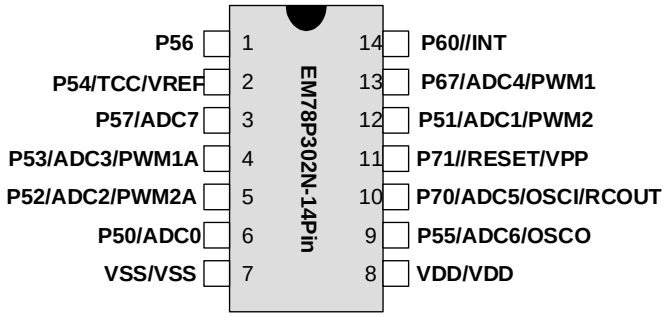


Figure 4-1 EM78P302N-14PIN

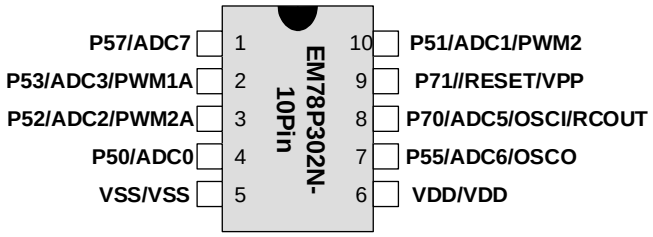


Figure 4-2 EM78P302N-10PIN

5 Block Diagram

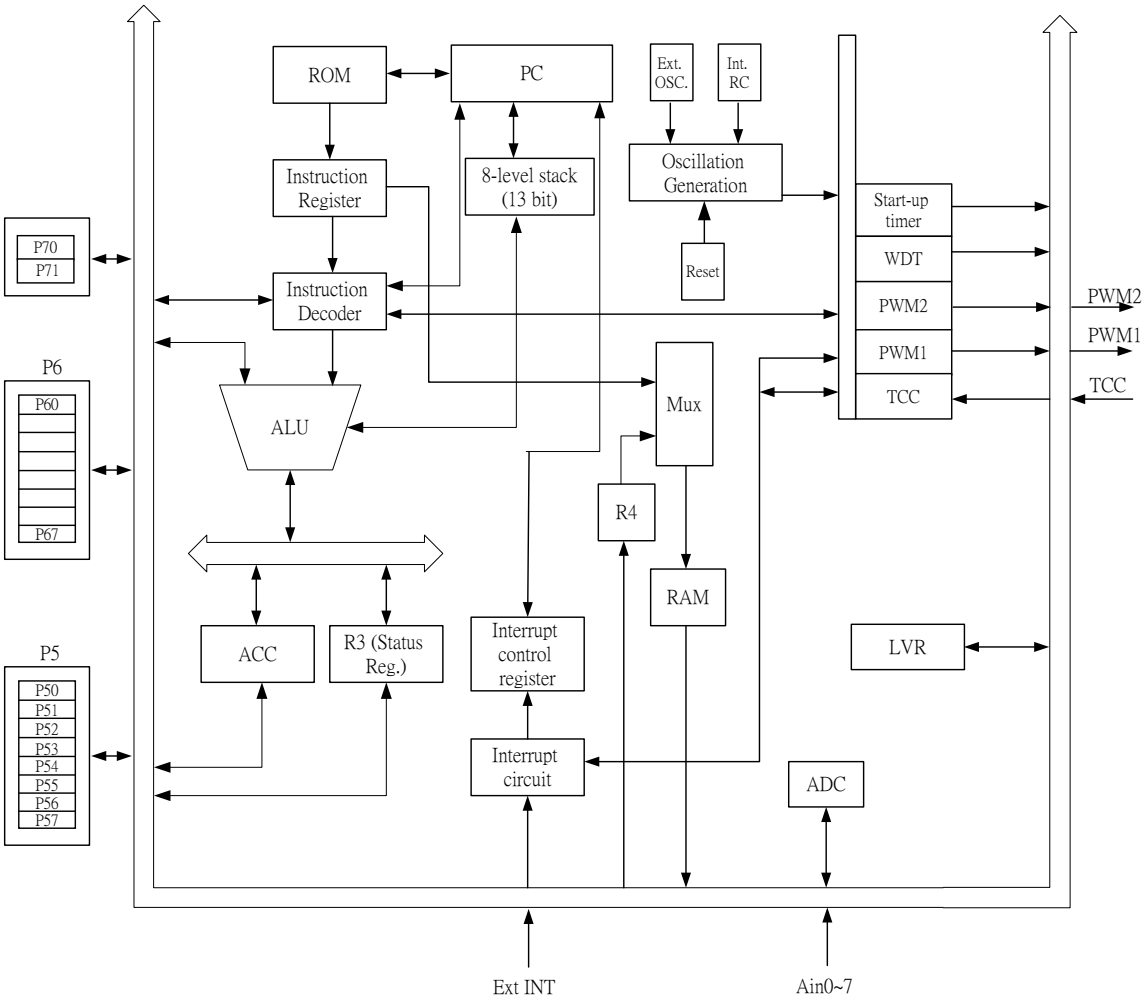


Figure 5-1 Functional Block Diagram

6 Pin Description

Name	Function	Input Type	Output Type	Description
P50/ADC0	P50	ST	CMOS	Bidirectional I/O pin with programmable pull- high, pull-low, and wake up pin from sleep mode when the status of the pin changes.
	ADC0	AN	–	Analog to Digital Converter input pins.
P51/ADC1/PWM2	P51	ST	CMOS	Bidirectional I/O pin with programmable pull- high, pull-low, and wake up pin from sleep mode when the status of the pin changes.
	ADC1	AN	–	Analog to Digital Converter input pins.
	PWM2	–	CMOS	Pulse width modulation output
P52/ADC2/PWM2A	P52	ST	CMOS	Bidirectional I/O pin with programmable pull- high, pull-low, and wake up pin from sleep mode when the status of the pin changes.
	ADC2	AN	–	Analog to Digital Converter input pins
	PWM2A		CMOS	Inverse PWM2 Output
P53/ADC3/PWM1A	P53	ST	CMOS	Bidirectional I/O pin with programmable pull- high, pull-low, and wake up pin from sleep mode when the status of the pin changes.
	ADC3	AN	–	Analog to Digital Converter input pins.
	PWM1A		CMOS	Inverse PWM1 Output
P54/TCC/VREF/ (ADPINOPT=0 : ADC4)	P54	ST	CMOS	Bidirectional I/O pin with programmable pull- high, pull-low, and wake up pin from sleep mode when the status of the pin changes.
	TCC	ST	–	Real Time Clock/Counter clock input.
	VREF	AN	–	External reference voltage for ADC.
	ADPINOPT1=0:ADC4 ADPINOPT1=1: N/A	AN	–	When ADPINOPT=0: Analog to Digital Converter input pins.
P55/ADC6/OSCO	P55	ST	CMOS	Bidirectional I/O pin with programmable pull- high, pull-low, and wake up pin from sleep mode when the status of the pin changes. **Remark: Off-chip pull-down or pull-high**
	ADC6	AN	–	Analog to Digital Converter input pins. **Remark: Off-chip pull-down or pull-high**
	OSCO	ST	–	Clock output of crystal/resonator oscillator

Name	Function	Input Type	Output Type	Description
P56	P56	ST	CMOS	Bidirectional I/O pin with programmable pull- high, pull-low, and wake up pin from sleep mode when the status of the pin changes
P57/ADC7	P57	ST	CMOS	Bidirectional I/O pin with programmable pull- high, pull-low, and wake up pin from sleep mode when the status of the pin changes.
	ADC7	AN	–	Analog to Digital Converter input pins.
P60//INT	P60	ST	CMOS	Bidirectional I/O pin with programmable pull-high, open-drain and wake up pin from sleep mode when the status of the pin changes.
	/INT	ST	–	External interrupt pin triggered by a falling edge
P67/(ADPINOPT=1:ADC4)/PWM1	P67	ST	CMOS	Bidirectional I/O pin with programmable pull-high, open-drain and wake up pin from sleep mode when the status of the pin changes.
	ADPINIOPT1=0: N/A ADPINIOPT1=1: ADC4	AN		ADPINOPT=1: Analog to Digital Converter input pin.
	PWM1	–	CMOS	Pulse width modulation output
P70/ADC5/OSCI/ RCOUT	P70	ST	CMOS	Bidirectional I/O pin
	ADC5	AN	–	Analog to Digital Converter input pins.
	OSCI	XTAL	–	Clock input of crystal/resonator oscillator
	RCOUT	–	CMOS	Clock output of internal RC oscillator
P71//RESET	P71	ST	CMOS	Bidirectional I/O pin (open-drain)
	/RESET	ST	–	External pull-high reset pin, active low.
VDD	VDD	Power	–	Power
VSS	VSS	Power	–	Ground

Legend: ST: *Schmitt Trigger input* ***AN****: analog pin*

XTAL*: oscillation pin for crystal/resonator* ***CMOS****: CMOS output*

NOTE

We strongly recommend that user has to place external pull-down or pull-high resistor (0Ω/1kΩ/ 10kΩ/100kΩ) on P55 no matter what the pin function is (except Crystal Mode). The purpose of this is to prevent P55 from floating.

7 Functional Description

7.1 Operational Registers

7.1.1 R0 (Indirect Addressing Register)

R0 is not a physically implemented register. Its major function is to perform as an indirect address pointer. Any instruction using R0 as a pointer, actually accesses the data pointed by the RAM Select Register (R4).

7.1.2 R1 (Timer Clock Counter)

R1 is incremented by an external signal edge, which is defined by the TE bit (CONT-4) through the TCC pin, or by the internal clock (Fm/Fs). It is writable and readable as any other registers. It is defined by resetting PSTE (CONT-3).

The prescaler is assigned to TCC, if the PSTE bit (CONT-3) is reset. The content of the prescaler counter is cleared only when the TCC register is written with a value.

7.1.3 R2 (Program Counter) and Stack

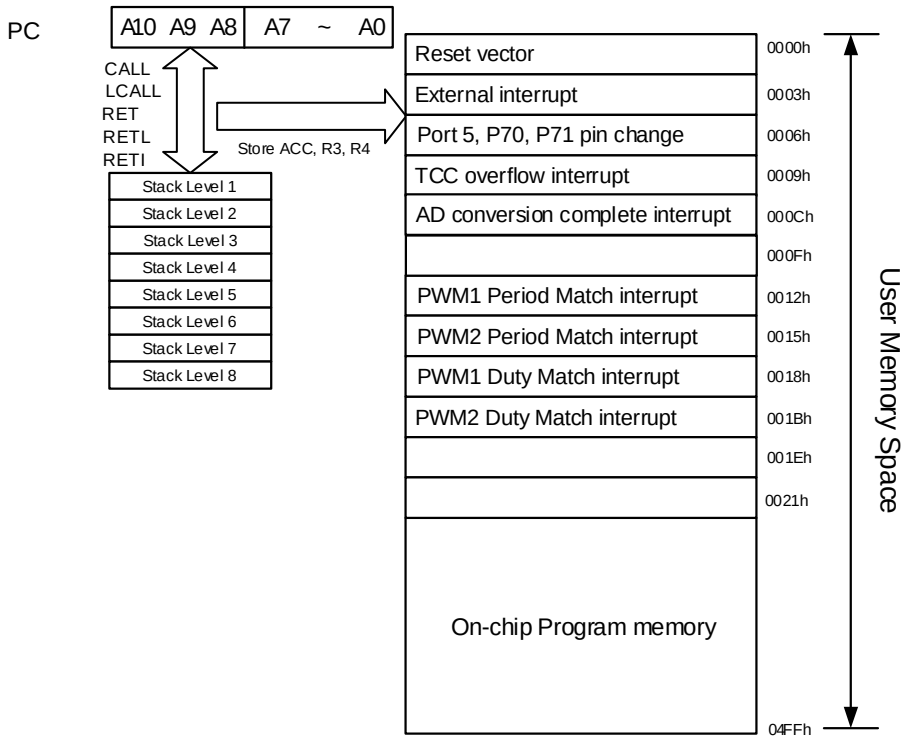


Figure 7-1 Program Counter Organization

- R2 and hardware stacks are 11-bit wide. The structure is depicted in Figure 7-1.
- Generates 1.25k ×13 bits on-chip ROM addresses to the relative programming instruction codes. One program page is 1024 words long.
- The contents of R2 are all set to "0"s when a RESET condition occurs.
- "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows PC to jump to any location within a page.
- "CALL" instruction loads the lower 10 bits of the PC, and then PC+1 is pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "LJMP" instruction allows direct loading of the program counter bits (A0~A10). Therefore, "LJMP" allows PC to jump to any location within 1.25k (2^{11})
- "LCALL" instruction loads the program counter bits (A0 ~A10), and then PC+1 is pushed onto the stack. Thus, the subroutine entry address can be located anywhere within 1.25k (2^{11})
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top of stack.
- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.
- "MOV R2, A" allows loading of an address from the "A" register to the lower 8 bits of the PC, and the ninth and above bits of the PC will remain unchanged.
- Any instruction (except “ADD R2, A”) that is written to R2 (e.g., "MOV R2, A", "BC R2, 6",·····) will cause the ninth bit and above bits (A8 ~ A10) of the PC to remain unchanged.
- All instructions are single instruction cycle (fclk/2 or fclk/4) except for the instructions that are written to R2.

Address	Register Bank 0	Register Bank 1	IOC Page 0	IOC Page 1
00	R0 (Indirect Addressing Register)			
01	R1 (Timer Clock Counter)			
02	R2 (Program Counter)			
03	R3 (Status Register)			
04	R4 (RSR, Bank select)			
05	R5 (Port 5 I/O data)	R5 (TBHP: Table Point Register)	IOC50 (Port 5 I/O control)	IOC51 (HSCR1: High Sink Control Register 1)
06	R6 (Port 6 I/O data)	R6 (TBLP: Table Point Register)	IOC60 (Port 6 I/O control)	IOC61 (HSCR2: High Sink Control Register 2)
07	R7 (Port 7 I/O data)	R7 (PWMCON: PWM Control Register)	IOC70 (Port 7 I/O control)	IOC71 (HDCR1: High Driver Control Register1)
08	R8 (ADC Input Select Register)	R8 (TMRCON: Timer Control Register)	IOC80 (Reserved)	IOC81 (HDCR2: High Driver Control Register 2)
09	R9 (ADC Control Register)	R9 (PRD1: PWM1 Time Period)	IOC90 (TMR1: PWM1 Timer)	IOC91 (DeadTCR: Dead Time Control Register)
0A	RA (ADC Offset Calibration Register)	RA (PRD2: PWM2 Time Period)	IOCA0 (TMR2: PWM2 Timer)	IOCA1 (DeadTR: Dead Time Register)
0B	RB (Converted value AD11~AD4 of ADC)	RB (DT1: PMW1 Duty Cycle)	IOCB0 (Pull-down Control Register)	IOCB1 (Pull-high Control Register)
0C	RC (Converted value AD11~AD8 of ADC)	RC (DT2: PMW2 Duty Cycle)	IOCC0 (Open-drain Control Register)	IOCC1 (Reserved)
0D	RD (Converted value AD7~AD0 of ADC)	RD (Reserved)	IOCD0 (Pull-high Control Register)	IOCD1 (Reserved)
0E	RE (Interrupt Status 2 and Wake-up Control Register 1)	RE (Wake-up Control Register 2)	IOCE0 (WDT Control Register and Interrupt Mask Register 2)	IOCE1 (Reserved)
0F	RF (Interrupt Status Register 1)	RF (Mode Select and IRC Switch Register)	IOCF0 (Interrupt Mask Register 1)	IOCF1 (Pull-high Control Register)
10 : 1F	16-Byte Common Register			
20 : 3F	Bank 0 32x8	Bank 1 32x8		

Figure 7-2 Data Memory Configuration

7.1.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RST	IOCS	-	T	P	Z	DC	C

Bit 7 (RST): Bit of reset type

Set to “1” if wake-up from sleep on pin change, comparator status change, External interrupt, Low Voltage Detector interrupt, or AD conversion completed. Set to “0” if wake-up from other reset types.

Bit 6 (IOCS): Select the Segment of I/O control register

0 = Segment 0 (IOC50 ~ IOCF0) selected

1 = Segment 1 (IOC51 ~ IOCF1) selected

Bit 5: Not used, set “0” at all time.

Bit 4 (T): Time-out bit. Set to “1” by the "SLEP" and "WDTC" commands or during power on**,** and reset to “0” by WDT time-out (for more details see Section 6.5.2, *The T and P Status under Status Register*).

Bit 3 (P): Power-down bit. Set to “1” during power-on or by a "WDTC" command and reset to “0” by a "SLEP" command (see Section 7.5.5, *The T and P Status under Status Register* for more details).

Bit 2 (Z): Zero flag. Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

7.1.5 R4 (RAM Select Register)

Bit 7 (SBANK):Special Register 0X05~0X0F Bank Selection Bit.

0 = SBANK 0

1 = SBANK 1

Bit 6: Used to select Bank 0 ~ Bank 1 of the register

Bits 5~0: Used to select a register (Address: 00~0F, 10~3F) in indirect addressing mode.

7.1.6 Bank 0 R5~R7 (Port 5~7 I/O Data Register)

R5~R6 and P70, P71 are I/O registers.

7.1.7 Bank 0 R8 (ADC Input Select Register)

The AISR register individually defines the I/O Port as analog input or as digital I/O.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0

Bit 7 (ADE7): AD converter enable bit of P57 pin

0 = Disable ADC7, P57 functions as I/O pin

1 = Enable ADC7 to function as analog input pin

Bit 6 (ADE6): AD converter enable bit of P55 pin

0 = Disable ADC6, P55 functions as I/O pin

1 = Enable ADC6 to function as analog input pin

Bit 5 (ADE5): AD converter enable bit of P70 pin

0 = Disable ADC5, P70 functions as I/O pin

1 = Enable ADC5 to function as analog input pin

Bit 4 (ADE4): **When ADPINOPT=0:**

AD converter enable bit of P54 pin

0 : Disable ADC4, P54 functions as I/O pin

1 : Enable ADC4 to function as analog input pin

When ADPINOPT=1:

AD converter enable bit of P67 pin

0 : Disable ADC4, P67 functions as I/O pin

1 : Enable ADC4 to function as analog input pin

Bit 3 (ADE3): AD converter enable bit of P53 pin

0 = Disable ADC3, P53 functions as I/O pin

1 = Enable ADC3 to function as analog input pin

Bit 2 (ADE2): AD converter enable bit of P52 pin

0 = Disable ADC2, P52 functions as I/O pin

1 = Enable ADC2 to function as analog input pin

Bit 1 (ADE1): AD converter enable bit of P51 pin

0 = Disable ADC1, P51 functions as I/O pin

1 = Enable ADC1 to function as analog input pin

Bit 0 (ADE0): AD converter enable bit of P50 pin

0 = Disable ADC0, P50 functions as I/O pin

1 = Enable ADC0 to function as analog input pin

NOTE

The P55/ADC6/OSCO pin cannot be applied to OSCO and ADC6 at the same time.

If P55/ADC6/OSCO functions as OSCO oscillator output pin, then ADE6 bit for R8 must be "0" and ADIS2~0 do not select "110". The P55/ADC6/OSCO pin priority is as follows:

P55/ADC6/OSCO Pin Priority		
High	Medium	Low
OSCO	ADC6	P55

The P70/ADC5/OSCI/RCOUT pin cannot be applied to OSCI and ADC5 at the same time.

If P70/ADC5/OSCI/RCOUT acts as OSCI oscillator input pin, then ADE5 bit for R8 must be "0" and ADIS2~0 do not select "101". The P70/ADC5/OSCI/RCOUT pin priority is as follows:

P70/ADC5/OSCI/RCOUT Pin Priority		
High	Medium	Low
OSCI/RCOUT	ADC5	P70

The P67/ADC4/PWM1 pin cannot be applied to PWM1 and ADC4 at the same time.

If P67/ADC4/PWM1 functions as ADC4 analog input pin, then the P67/ADC4/PWM1 pin priority is as follows:

P67/ADC4/PWM1 Pin Priority		
High	Medium	Low
ADC4	PWM1	P67

The P51/ADC1/PWM2 pin cannot be applied to PWM2 and ADC1 at the same time.

If P51/ADC1/PWM2 functions as ADC1 analog input pin, then the P51/ADC1/PWM2 pin priority is as follows:

P51/ADC1/PWM2 Pin Priority		
High	Medium	Low
ADC1	PWM2	P51

The P50/ADC0 pin cannot be applied to I/O and ADC0 at the same time.

If P50/ADC0 functions as ADC0 analog input pin, then the P50/ADC0 pin priority is as follows:

P50/ADC0 Pin Priority	
High	Low
ADC0	P50

7.1.8 Bank 0 R9 (ADC Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VREFS	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0

Bit 7 (VREFS): The input source of Vref of the ADC

0 : The Vref of the ADC is connected to internal reference voltage (default value), and the P54/TCC/VREF/(ADPINOPT=0: ADC4) pin carries out the function of P54.

1 : The Vref of the ADC is connected to P54/TCC/VREF/(ADPINOPT=0:ADC4)

NOTE

- *The P54/TCC/VREF/(ADPINOPT=0:ADC4) pin cannot be applied to TCC, ADC4 and VREF at the same time. If P54/TCC/VREF/(ADPINOPT=0:ADC4) functions as VREF analog input pin, then CONT Bit 5 "TS" must be "0".*
- *The P54/TCC/VREF/(ADPINOPT=0:ADC4) Pin Priority is as follows:*

P54/TCC/ADC4/VREF Pin Priority		
High	Medium	Low
VREF/ADC4	TCC	P54

Bit 6 and Bit 5 (CKR1 and CKR0): The prescaler of ADC oscillator clock rate

CPUS	CKR1 : CKR0	Operation Mode	Max. Operation Frequency (if TAD=4μs, match 372N)	Max. Operation Frequency (if TAD=1μs, match 372N)
1	00 (default)	$F_{OSC}/16$	4 MHz	16 MHz
1	01	$F_{OSC}/4$	1 MHz	4 MHz
1	10	$F_{OSC}/64$	16 MHz	-
1	11	$F_{OSC}/1$	-	1 MHz
0	××	-	16K/128kHz	16K/128kHz

Bit 4 (ADRUN): ADC starts to RUN

0: Reset upon completion of the conversion. This bit cannot be reset through software

1: AD conversion is started. This bit can be set by software.

Bit 3 (ADPD): ADC Power-down mode

0: Switch off the resistor reference to save power even while the CPU is operating.

1: ADC is operating

Bits 2 ~ 0 (ADIS2 ~ ADIS0): Analog Input Select

ADICS	ADIS2	ADIS1	ADIS0	Analog Input Select
0	0	0	0	ADC0 / P50
0	0	0	1	ADC1 / P51
0	0	1	0	ADC2 / P52
0	0	1	1	ADC3 / P53
0	1	0	0	ADIN4 / (ADPINOPT=0:P54) or (ADPINOPT=1:P67)
0	1	0	1	ADC5 / P70
0	1	1	0	ADC6 / P55
0	1	1	1	ADC7 / P57
1	1	0	0	Internal ADC Channel Select: 1/4 VDD
1	1	0	1	Internal ADC Channel Select: 1 / 2 VDD
1	1	1	0	Reserved
1	1	1	1	Reserved

7.1.9 Bank 0 RA (ADC Offset Calibration Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	VREF1	VREF0	ADICS

Bit 7 (CALI): Calibration enable bit for ADC offset

0: Disable the Calibration

1: Enable the Calibration

Bit 6 (SIGN): Polarity bit of offset voltage

0: Negative voltage

1: Positive voltage

Bit 5 ~ Bit 3 (VOF[2] ~ VOF[0]): Offset voltage bits

VOF[2]	VOF[1]	VOF[0]	EM78P302N
0	0	0	0 LSB
0	0	1	2 LSB
0	1	0	4 LSB
0	1	1	6 LSB
1	0	0	8 LSB
1	0	1	10 LSB
1	1	0	12 LSB
1	1	1	14 LSB

Bits 2 ~ 1 (VREF1 ~ VREF0): ADC internal reference voltage source.

VREFSEL in Option Word 3 Bit 11	VREF[1]	VREF[0]	ADC Int. Ref. Volt
0	0	0	VDD
0	0	1	4.0V ± 1%
0	1	0	3.0V ± 1%
0	1	1	2.5V ± 1%
1	0	0	VDD
1	0	1	4.0V ± 1%
1	1	0	3.0V ± 1%
1	1	1	2.0V ± 1%

If VREF[1:0]＝00, internal reference doesn't turn on. If VREF[1:0]≠00, internal reference will turn on automatically. Moreover, the power of internal reference is irrelevant to power of ADC. That means one of VREF[1:0] is set, the internal reference turns on.
If VREF[1:0]＝11, internal reference will turn on by code option selected with VREF 2.0V or VREF 2.5V.

Bit 0 (ADICS): ADC internal channel select**.** (Select ADC internal 1/4 VDD or 1/2VDD connects to ADC input)

0 = Disable

1 = Enable

7.1.10 Bank 0 RB (Converted Value AD11~AD4 of ADC)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4

When AD conversion is completed, the result is loaded into the ADDATA. The ADRUN bit is cleared and the ADIF is set.

RB is read only.

7.1.11 Bank 0 RC (Converted Value AD11~AD8 of ADC)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	AD11	AD10	AD9	AD8

When AD conversion is completed, the result is loaded into the ADDATA1H. The ADRUN bit is cleared and the ADIF is set.

RC is read only.

7.1.12 Bank 0 RD (Converted Value AD7~AD0 of ADC)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

When AD conversion is completed, the result is loaded into the ADDATA1L. The ADRUN bit is cleared and the ADIF is set.

RD is read only

7.1.13 Bank 0 RE (Interrupt Status 2 and Wake-up Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	ADIF	-	ADWE	-	ICWE	-

Note: *1. RE <5> can be cleared by instruction but cannot be set.*
2. IOCE0 is the interrupt mask register.
3. Reading RE will result to "Logic AND" of the RE and IOCE0.

Bit 7: Not used, set to "1" at all time.

Bit 6: Not used, set to "0" at all time.

Bit 5 (ADIF): Interrupt flag for Analog to Digital conversion. Set when AD conversion is completed. Reset by software.

0 : No interrupt occurs

1 : With interrupt request

Bit 4 : Not used. Set “0” at all the time

Bit 3 (ADWE): ADC wake-up enable bit

0 : Disable ADC wake-up

1 : Enable ADC wake-up

When AD Conversion enters sleep/idle mode, this bit must be set to “Enable”.

Bit 2 : Not used. Set “0” at all the time

Bit 1 (ICWE): Port 5, P70, and P71 input change to wake-up status enable bit

0 : Disable Port 5, P70, P71 input change to wake-up status

1 : Enable Port 5, P70, P71 input change to wake-up status

When Port 5, P70, P71 change enters sleep/idle mode, this bit must be set to “Enable”.

Bit 0: Not used, set to “0” at all time.

7.1.14 Bank 0 RF (Interrupt Status Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P7ICIF	DT2IF	DT1IF	PWM2IF	PWM1IF	EXIF	ICIF	TCIF

Note: *1. “1” means there is an interrupt request, “0” means no interrupt occurs.*
2. RF can be cleared by instruction but cannot be set.
3. IOCF0 is the interrupt mask register.
4. Reading RF will result to “Logic AND” of the RF and IOCF0.

Bit 7 (P7ICIF): Port 7 input status change interrupt flag. Set when Port 7 input changes. Reset by software.

Bit 6 (DT2IF): PWM2 duty match interrupt flag. Reset by software.

Bit 5 (DT1IF): PWM1 duty match interrupt flag. Reset by software.

Bit 4 (PWM2IF): PWM2 period match interrupt flag. Reset by software.

Bit 3 (PWM1IF): PWM1 period match interrupt flag. Reset by software.

Bit 2 (EXIF): External interrupt flag. Set by falling edge on /INT pin. Reset by software.

Bit 1 (ICIF): Port 5 input status change interrupt flag. Set when Port 5 input changes. Reset by software.

Bit 0 (TCIF): TCC overflow interrupt flag. Set when TCC overflows. Reset by software.

7.1.15 Bank 1 R5 (TBHP: Table Point Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MLB	TRS	-	-	RBit11	RBit10	RBit9	RBit8

Bit 7 (MLB): Choosing MSB or LSB machine code to be moved to the register.

The machine code is pointed by TBLP and TBHP register.

Bit 6 (TRS): Table Read Select

0: read ROM

1: read Customer ID Register

NOTE

When TRS = 1 (read Customer ID Register)

- *Can read Customer ID Register II, III (Word 0x10 or Word 0x11)*
- *Cannot read Customer ID Register I (Word 2)*
- *Don't care RBit11 ~ RBit3*

Bits 5~4: Not used, set to "0" at all time.

Bits 3~0: These are the most 4 significant bits of address for program code.

7.1.16 Bank 1 R6 (TBLP: Table Point Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBit7	RBit6	RBit5	RBit4	RBit3	RBit2	RBit1	RBit0

Bits 7 ~ 0 (RBit7~RBit0): Table point low byte bits.

When TRS = 0 (Read ROM):

RBit7~RBit0 are the least 8 significant bits of address for program code.

When TRS = 1 (Read Customer ID Register):

RBit7	RBit6	RBit5	RBit4	RBit3	RBit2	RBit1	RBit0	Customer ID
x	x	x	x	x	0	0	0	Word 0x10
x	x	x	x	x	0	0	1	Word 0x11
x	x	x	x	x	0	1	x	Reserved
x	x	x	x	x	1	x	x	Reserved

NOTE

- *Bank 1 R6 overflow will carry to Bank 1 R5.*
- *Bank 1 R6 underflow will borrow from Bank 1 R5.*

7.1.17 Bank 1 R7 (PWMCON: PWM Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IPWM2E	IPWM1E	-	-	-	PWMCAS	PWM2E	PWM1E

Bit 7 (IPWM2E): Inverse PWM2 Enable bit

0: Inverse PWM2 is off (default value), and its related pin carries out the P52 function.

1: Inverse PWM2 is on, and its related pin is automatically set to output.

Bit 6 (IPWM1E): Inverse PWM1 Enable bit

0: Inverse PWM1 is off (default value), and its related pin carries out the P53 function.

1: Inverse PWM1 is on, and its related pin is automatically set to output.

Bits 5 ~ 3: Not used

Bit 2 (PWMCAS): PWM Cascade Mode

0: Two Independent 8-bit PWM function (default value)

1: 16-bit PWM Mode (Cascaded from two 8-bit ones)

Bit 1 (PWM2E): PWM2 Enable bit

0: PWM2 is off (default value), and its related pin carries out the P67 function.

1: PWM2 is on, and its related pin is automatically set to output.

Bit 0 (PWM1E): PWM1 Enable bit

0: PWM1 is off (default value), and its related pin carries out the P51 function.

1: PWM1 is on, and its related pin is automatically set to output.

7.1.18 Bank 1 R8 (TMRCON: Timer Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T2EN	T1EN	T2P2	T2P1	T2P0	T1P2	T1P1	T1P0

Bit 7 (T2EN): TMR2 Enable bit

0: TMR2 is off (default value)

1: TMR2 is on

Bit 6 (T1EN): TMR1 Enable bit

0: TMR1 is off (default value)

1: TMR1 is on

Bit 5 ~ Bit 3 (T2P2 ~ T2P0): TMR2 clock prescaler option bits

T2P2	T2P1	T2P0	Prescale
0	0	0	1:1 (default)
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 2 ~ Bit 0 (T1P2 ~ T1P0): TMR1 clock prescaler option bits

T1P2	T1P1	T1P0	Prescale
0	0	0	1:1 (default)
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

7.1.19 Bank 1 R9 (PRD1: PWM1 Time Period)

The content of Bank 1-R9 is the time period (time base) of PWM1. The frequency of PWM1 is the reverse of the period.

7.1.20 Bank 1 RA (PRD2: PWM2 Time Period)

The content of Bank 1-RA is the time period (time base) of PWM2. The frequency of PWM2 is the reverse of the period.

7.1.21 Bank 1 RB (DT1: PWM1 Duty Cycle)

A specified value keeps the output of PWM1 to remain high until the value matches with TMR1.

7.1.22 Bank 1 RC (DT2: PWM2 Duty Cycle)

A specified value keeps the output of PWM2 to remain high until the value matches with TMR2.

7.1.23 Bank 1 RE (Wake-up Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	-	EXWE

Bits 7~1: Not used, set to "0" at all time.

Bit 0 (EXWE): External /INT wake-up enable bit

0: Disable External /INT pin wake-up

1: Enable External /INT pin wake-up

7.1.24 Bank 1 RF (Mode Select and IRC Switch Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	TIMERSC	CPUS	IDLE	SHS1	SHS0	RCM1	RCM0

Bit 7: Not used. Set "0" all the time.

Bit 6 (TIMERSC): TCC, PWM1, PWM2 clock sources select 0/1 → Fs/Fm*

0 : Fs: Sub-oscillator clock from WDT 16kHz ± 30% or System hold RC 128kHz ± 30%(determined by Word 2 SFS bit)

1 : Fm: main-oscillator clock

Bit 5 (CPUS): CPU Oscillator Source Select

0 : Sub-oscillator (Fs)

1 : Main-oscillator (Fm)

When CPUS=0, the CPU oscillator selects the sub-oscillator and the main oscillator is stopped.

Bit 4 (IDLE): Idle Mode Enable Bit. From SLEP instruction, this bit will determine as to which mode to go.

0 : Idle= "0"+SLEP instruction → sleep mode

1 : Idle= "1"+SLEP instruction → idle mode

Bits 3 ~ 2 (SHS1~0): Select AD sample and hold period.

SHS1	SHS0	AD Sample and Hold Period (TAD)
0	0	2
0	1	4
1	0	8
1	1	12 (default)

CPU Operation Mode

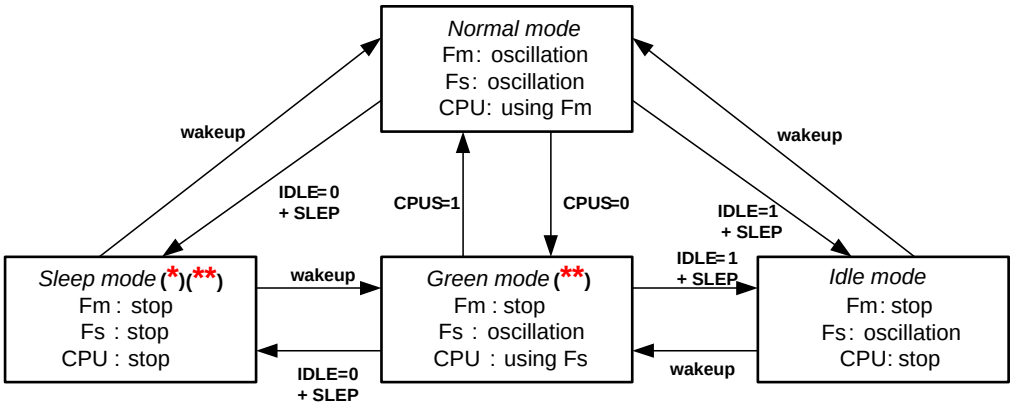


Figure 7-4 CPU Operation Mode

(*)

If the Watchdog function is enabled before going into sleep mode, some circuits like the Timer (its clock source is Fs) must stop counting.

If the Watchdog function is enabled before going into sleep mode, some circuits like the Timer (its clock source is an external pin) can still count and its Interrupt flag can be active at matching conditions, as corresponding interrupt is enabled. But CPU cannot be awakened by this event.

(**)

Switching Operation Mode from Sleep → Normal, Green → Normal

If the clock source of the Timer is Fm, the Timer/Counter must stop counting at Sleep or Green mode. Then the Timer can continue to count until the clock source is stable at Normal mode. That the clock source is stable means that the CPU starts to work at Normal mode.

Switching Operation Mode from Sleep → Green

If the clock source of the Timer is Fs, the Timer must stop counting at Sleep mode. Then the Timer can continue to count until the clock source is stable at Green mode. That the clock source is stable means that the CPU starts to work at Green mode.

Switching Operation Mode from Sleep → Normal

If the clock source of the Timer is Fs, the Timer must stop counting at Sleep mode. Then the Timer can continue to count until the clock source is stable at Normal mode. That the clock source is stable means that the CPU starts to work at Normal mode.

NOTE

■ *Crystal MOD1 for LXT1, XT, HXT2, HXT1:*

Sleep → Normal = Oscillator Stable Time + 510 clocks (main frequency).

Sleep → Green = Oscillator Stable Time + 8 clocks (sub frequency).

Green → Normal = Oscillator Stable Time + 510 clocks (main frequency)

■ *Crystal MOD2 for LXT2 :*

Sleep → Normal = Oscillator Stable Time + 254 clocks (main frequency).

Sleep → Green = Oscillator Stable Time + 8 clocks (sub frequency).

Green → Normal = Oscillator Stable Time + 254 clocks (main frequency)

■ *IRC MOD :*

Sleep → Normal = Oscillator Stable Time + 8 or 32 clocks (main frequency).

Sleep → Green = Oscillator Stable Time + 8 clocks (sub frequency).

Green → Normal = Oscillator Stable Time + 8 clocks (main frequency)

Bits 3~2: Not used, set to “0” at all time.

Bits 1~0 (RCM1: 0): IRC mode selection bits

RCM 1	RCM 0	*Frequency (MHz)
1	1	4
1	0	16
0	1	8
0	0	1

NOTE

■ *Word 2<11> COBS0=0 :*

Bank 1 RF<1~0> of the initialized values will be kept the same as Word 1<6~5>.

Bank 1 RF<1~0> cannot change

■ *Word 2<11> COBS0=1 :*

Bank 1 RF<1~0> of the initialized values will be kept the same as Word 1<6~5>.

Bank 1 RF<1~0> can change, When user wants to work on other IRC frequency.

Stable time is 8 clocks

7.1.25 R10~R1F

All of these are 8-bit general-purpose registers.

7.2 Special Purpose Registers

7.2.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator, which is not an addressable register.

7.2.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE	INT	TS	TE	PSTE	PST2	PST1	PST0

Note: *The CONT register is both readable and writable.*
Bit 6 is read only.

Bit 7 (INTE): INT signal edge

0 : Interrupt occurs at a rising edge of the INT pin

1 : Interrupt occurs at a falling edge of the INT pin

Bit 6 (INT): Interrupt Enable flag

0 : Masked by DISI or hardware interrupt

1 : Enabled by the ENI/RETI instructions

This bit is readable only.

Bit 5 (TS): TCC signal source

0 : Internal instruction cycle clock. If P54 is used as I/O pin

1 : Transition on the TCC pin

Bit 4 (TE): TCC signal edge

0 : Increment if the transition from low to high takes place on the TCC pin

1 : Increment if the transition from high to low takes place on the TCC pin.

Bit 3 (PSTE): Prescaler enable bit for TCC

0 = prescaler disable bit. TCC rate is 1:1.

1 = prescaler enable bit. TCC rate is set at Bit 2 ~ Bit 0.

Bit 2 ~ Bit 0 (PST2 ~ PST0): TCC prescaler bits

PST2	PST1	PST0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Note:

$$TCC\ Timeout\ period\ =\ \frac{1}{FT}\ \times\ \left(256-TCC\ cnt\right)\times\ 1\ ,$$

where $FT = Fm\ or\ Fs$, *decide by BANK*1 *RF TIMERSCbit.*

7.2.3 IOC50 ~ IOC70 (I/O Port Control Register)

"**0**" defines the relative I/O pin as output

"**1**" sets the relative I/O pin into high impedance

7.2.4 IOC90 (TMR1: PWM1 Timer)

7.2.5 IOCA0 (TMR2: PWM2 Timer)

7.2.6 IOCB0 (Pull-down Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PD57	/PD56	/PD55	/PD54	/PD53	/PD52	/PD51	/PD50

The **IOCB0** register is both readable and writable.

Bit 7 (/PD57): Control bit used to enable internal pull-down of the P57 pin.

0 : Enable internal pull-down

1 : Disable internal pull-down

Bit 6 (/PD56): Control bit used to enable internal pull-down of the P56 pin.

Bit 5 (/PD55): Control bit used to enable internal pull-down of the P55 pin.

Bit 4 (/PD54): Control bit used to enable internal pull-down of the P54 pin.

Bit 3 (/PD53): Control bit used to enable internal pull-down of the P53 pin.

Bit 2 (/PD52): Control bit used to enable internal pull-down of the P52 pin.

Bit 1 (/PD51): Control bit used to enable internal pull-down of the P51 pin.

Bit 0 (/PD50): Control bit used to enable internal pull-down of the P50 pin.

7.2.7 IOCC0 (Open-drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD67	-	-	-	-	-	-	OD60

The IOCC0 register is both readable and writable.

Bit 7 (OD67): Control bit used to enable open-drain output of the P67 pin.

0 : Disable open-drain output

1 : Enable open-drain output

Bits 6~1: Not used.

Bit 0 (OD60): Control bit used to enable open-drain output of the P60 pin.

7.2.8 IOCD0 (Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH57	/PH56	/PH55	/PH54	/PH53	/PH52	/PH51	/PH50

The **IOCD0** register is both readable and writable.

Bit 7 (/PH57): Control bit used to enable internal pull-high of the P57 pin.

0 = Enable internal pull-high

1 = Disable internal pull-high

Bit 6 (/PH56): Control bit used to enable internal pull-high of the P56 pin.

Bit 5 (/PH55): Control bit used to enable internal pull-high of the P55 pin.

Bit 4 (/PH54): Control bit used to enable internal pull-high of the P54 pin.

Bit 3 (/PH53): Control bit used to enable internal pull-high of the P53 pin.

Bit 2 (/PH52): Control bit used to enable internal pull-high of the P52 pin.

Bit 1 (/PH51): Control bit used to enable internal pull-high of the P51 pin.

Bit 0 (/PH50): Control bit used to enable internal pull-high of the P50 pin.

7.2.9 IOCE0 (WDT Control Register and Interrupt Mask Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	ADIE	-	PSWE	PSW2	PSW1	PSW0

Bit 7 (WDTE): Control bit used to enable Watchdog Timer

0 : Disable WDT

1 : Enable WDT

WDTE is both readable and writable.

Bit 6 (EIS): Control bit used to define the function of the P60 (/INT) pin

0 : P60, bidirectional I/O pin

1 : /INT, external interrupt pin. In this case, the I/O control bit of P60 (Bit 0 of IOC60) must be set to "1".

NOTE

- *When EIS is "0", the path of /INT is masked. When EIS is "1", the status of the /INT pin can also be read by way of reading Port 6 (R6).*
- *EIS is both readable and writable.*

Bit 5 (ADIE): ADIF interrupt enable bit

0 : disable ADIF interrupt

1 : enable ADIF interrupt

Bit 4 : Not used.

Bit 3 (PSWE): Prescaler enable bit for WDT

0 : prescaler disable bit, WDT rate is 1:1

1 : prescaler enable bit, WDT rate is set as Bit 2 ~ Bit 0

Bit 2 ~ Bit 0 (PSW2 ~ PSW0): WDT prescaler bits

PSW2	PSW1	PSW0	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

7.2.10 IOCF0 (Interrupt Mask Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P7ICIE	DT2IE	DT1IE	PWM2IE	PWM1IE	EXIE	ICIE	TCIE

Note: *The IOCF0 register is both readable and writable.*

Individual interrupt is enabled by setting to "1" its associated control bit in the IOCF0 and bit 5 in IOCE0.

Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction.

Bit 7 (P7ICIE): P7ICIF interrupt enable bit

0 : Disable ICIF interrupt

1 : Enable ICIF interrupt

Bit 6 (DT2IE): DT2IF interrupt enable bit

0 : Disable DT2IF interrupt

1 : Enable DT2IF interrupt

Bit 5 (DT1IE): DT1IF interrupt enable bit

0 : Disable DT1IF interrupt

1 : Enable DT1IF interrupt

Bit 4 (PWM2IE): PWM2IF interrupt enable bit

0 : Disable PWM2IF interrupt

1 : Enable PWM2IF interrupt

Bit 3 (PWM1IE): PWM1IF interrupt enable bit

0 : Disable PWM1IF interrupt

1 : Enable PWM1IF interrupt

Bit 2 (EXIE): EXIF interrupt enable bit

0 : Disable EXIF interrupt

1 : Enable EXIF interrupt

Bit 1 (ICIE): ICIF interrupt enable bit

0 : Disable ICIF interrupt

1 : Enable ICIF interrupt

Bit 0 (TCIE): TCIF interrupt enable bit.

0 : Disable TCIF interrupt

1 : Enable TCIF interrupt

7.2.11 IOC51 (HSCR1: High Sink Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HS57	HS56	HS55	HS54	HS53	HS52	HS51	HS50

Bit 7 (HS57): Output High Sink Current Select for P57

Bit 6 (HS56): Output High Sink Current Select for P56

Bit 5 (HS55): Output High Sink Current Select for P55

Bit 4 (HS54): Output High Sink Current Select for P54

Bit 3 (HS53): Output High Sink Current Select for P53

Bit 2 (HS52): Output High Sink Current Select for P52

Bit 1 (HS51): Output High Sink Current Select for P51

Bit 0 (HS50): Output High Sink Current Select for P50

HSxx	VDD = 5V, Sink Current
0	12 mA (in 0.1VDD)
1	25 mA (in 0.1VDD)

7.2.12 IOC61 (HSCR2: High Sink Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HS67	-	-	-	-	-	-	HS60

Bit 7 (HS67): Output High Sink Current Select for P67

Bit 6~1 : Not used

Bit 0 (HS60): Output High Sink Current Select for P60

HSxx	VDD = 5V, Sink Current
0	12 mA (in 0.1VDD)
1	25 mA (in 0.1VDD)

7.2.13 IOC71 (HDCR1: High Driver Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HD57	HD56	HD565	HD54	HD53	HD52	HD51	HD560

Bit 7 (HD57): Output High Driver Current Select for P57

Bit 6 (HD56): Output High Driver Current Select for P56

Bit 5 (HD55): Output High Driver Current Select for P55

Bit 4 (HD54): Output High Driver Current Select for P54

Bit 3 (HD53): Output High Driver Current Select for P53

Bit 2 (HD52): Output High Driver Current Select for P52

Bit 1 (HD51): Output High Driver Current Select for P51

Bit 0 (HD50): Output High Driver Current Select for P50

HDxx	VDD = 5V, Drive Current
0	6 mA (in 0.9VDD)
1	18 mA (in 0.9VDD)

7.2.14 IOC81 (HDCR2: High Driver Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HD67	-	-	-	-	-	-	HD60

Bit 7 (HD67): Output High Driver Current Select for P67

Bits 6~1: Not used

Bit 0 (HD60): Output High Driver Current Select for P60

HDxx	VDD = 5V, Driver Current
0	6 mA (in 0.9VDD)
1	18 mA (in 0.9VDD)

7.2.15 IOC91 (DeadTCR: Dead Time Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IPWM2A	IPWM1A	PWM2A	PWM1A	DEADT2E	DEADT1E	-	-
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0

Bit 7 (IPWM2A): active level of inverse PWM2

0: period-duty-dead time is Logic 1 (default)

1: period-duty-dead time is Logic 0

Bit 6 (IPWM1A): active level of inverse PWM1

0: period-duty-dead time is Logic 1 (default)

1: period-duty-dead time is Logic 0

Bit 5 (PWM2A): Active level of PWM2

0: duty-dead time is Logic 1 (default)

1: duty-dead time is Logic 0

Bit 4 (PWM1A): Active level of PWM1

0: duty-dead time is Logic 1 (default)

1: duty-dead time is Logic 0

Bit 3 (DEADT2E): Enable dead time function for PWM2 and /PWM2 (for dual PWM)

0: Disable (default)

1: Enable

Bit 2 (DEADT1E): Enable dead time function for PWM1 and /PWM1 (for dual PWM)

0: Disable (default)

1: Enable

Bits 1~0: Not used, set to "0" at all time

NOTE

The deadtime function is only for dual PWM. If using single PWM function (not dual PWM), the deadtime function is always disabled.

7.2.16 IOCA1 (DeadTR: Dead Time Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	DEADTR3	DEADTR2	DEADTR1	DEADTR0
R-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0

Bits 7 ~ 4: Not used, set to "0" at all time.

Bits 3~0 (DEADTR3~0): The content of the register is dead time.

NOTE

The value in dead-time register must be less than the value in duty cycle register, in order to prevent unexpected behavior on both of PWM outputs.

7.2.17 IOCB1 (Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	-	/PH70
R-1	R-1	R-1	R-1	R-1	R-1	R-1	R/W-1

Bits 7 ~ 1: Not used, set to "1" at all time.

Bit 0 (/PH70): Control bit used to enable pull-high of the P70 pin.

0 = Enable internal pull-high

1 = Disable internal pull-high

7.2.18 IOCF1 (Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH67	-	-	-	-	-	-	/PH60

Note: *The IOCD0 register is both readable and writable.*

Bit 7 (/PH67): Control bit used to enable pull-high of the P67 pin.

0 = Enable internal pull-high

1 = Disable internal pull-high

Bits 6 ~ 1: Not used.

Bit 0 (/PH60): Control bit used to enable internal pull-high of the P60 pin.

7.3 TCC/WDT and Prescaler

There are two 8-bit counters available as prescalers for the TCC and WDT respectively. The PST2 ~ PST0 bits of the CONT register are used to determine the ratio of the TCC prescaler, and the PSW2 ~ PSW0 bits of the IOCE0 register are used to determine the prescaler of WDT. The prescaler counter is cleared by the instructions each time such instructions are written into TCC. The WDT and prescaler will be cleared by the "WDTC" and "SLEP" instructions. Figure 7-5 depicts the block diagram of TCC/WDT.

TCC (R1) is an 8-bit timer/counter. The TCC clock source can be an internal clock (Fm/Fs) or external signal input (edge selectable from the TCC pin). If TCC signal source is from the internal clock (Fm/Fs), TCC will increase by 1 at every Fm clock or Fs clock (without prescaler), decide by Bank 1 RF TIMERSC bit. If TCC signal source is from an external clock input, TCC will increase by 1 at every falling edge or rising edge of the TCC pin. The TCC pin input time length (kept in High or Low level) must be greater than Fm clock or Fs clock, determined by Bank 1 RF CPUS bit.

NOTE

The internal TCC will stop running when in sleep mode. However, during AD conversion, when TCC is set to "SLEP" instruction, if the ADWE bit of the RE register is enabled, the TCC will keep on running.

Usage of TCC function

```
Interrupt
    1. Reload TCC (R1)
        MOV   A, @ k
        MOV   TCC, A
    2. Reset TCC overflow interrupt flag
        BC      TCIF
```

NOTE

You must reload TCC (R1) before reset TCC overflow interrupt flag.

The Watchdog Timer is a free running on-chip RC oscillator. The WDT will keep on running even when the oscillator driver has been turned off (i.e., in sleep mode). During normal operation or in sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled any time during normal mode through software programming. With no prescaler, the WDT time-out period is approximately 18ms[1] or 4.5ms[2].

[1] VDD=5V, WDT time-out period = 16.5ms ± 30%
VDD=3V, WDT time-out period = 18ms ± 30%

[2] VDD=5V, WDT time-out period = 4.2ms ± 30%
VDD=3V, WDT time-out period = 4.5ms ± 30%

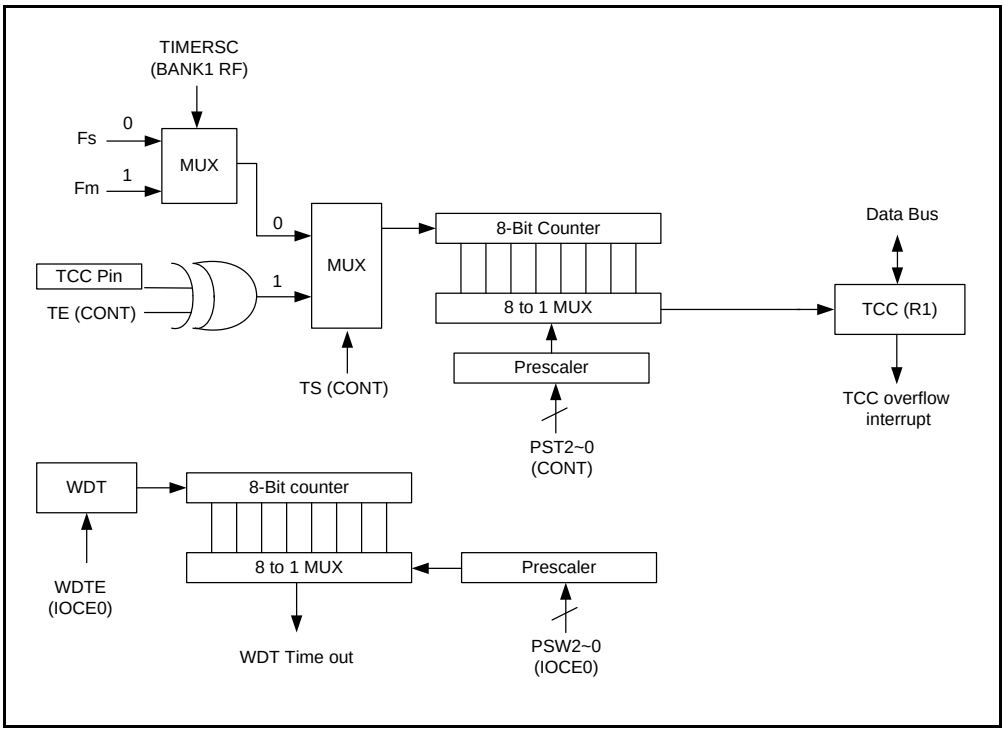
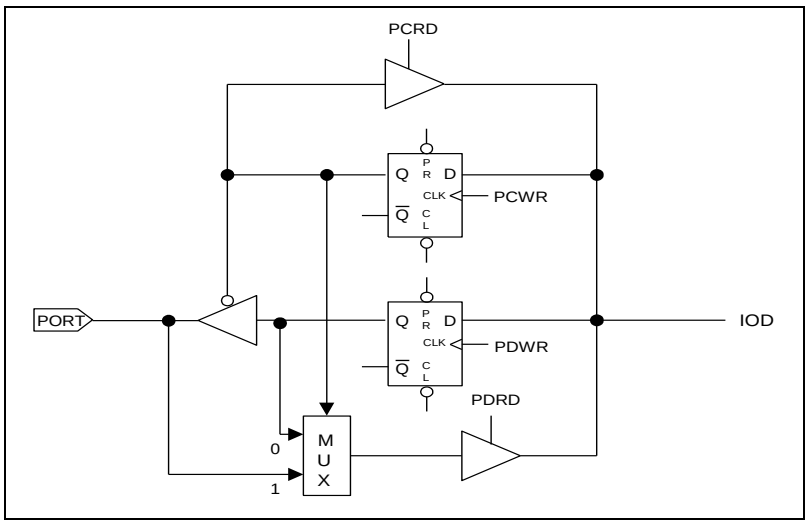


Figure 7-5 TCC and WDT Block Diagram

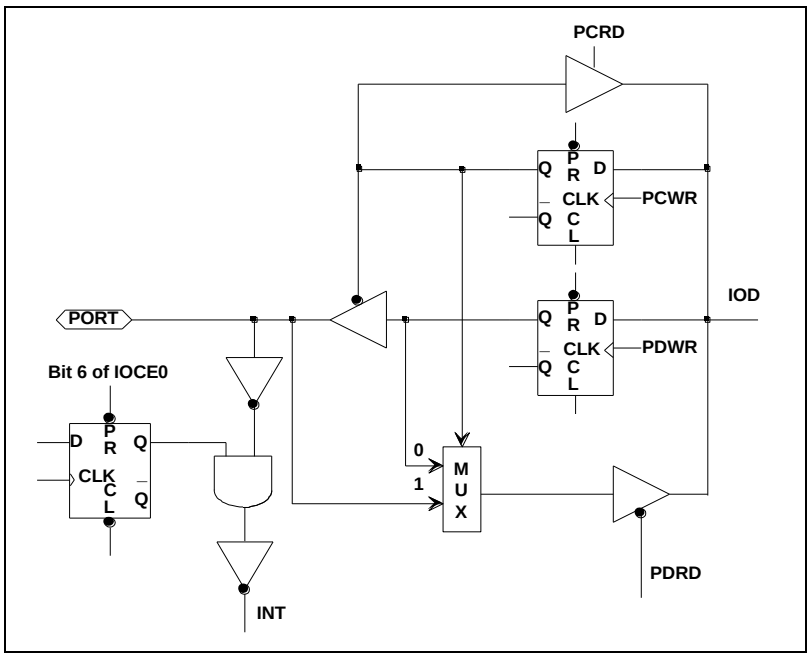
7.4 I/O Ports

The I/O registers (Port 5, Port 6, and Port 7) are bidirectional tri-state I/O ports. Port 5 is pulled-high and pulled-down internally by software. Likewise, P6 has its open-drain output set through software. Port 5 features an input status changed interrupt (or wake-up) function. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC50 ~ IOC70). The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5, Port 6, and Port 7 are illustrated in Figures 7-6, 7-7, 7-8, and 7-9.



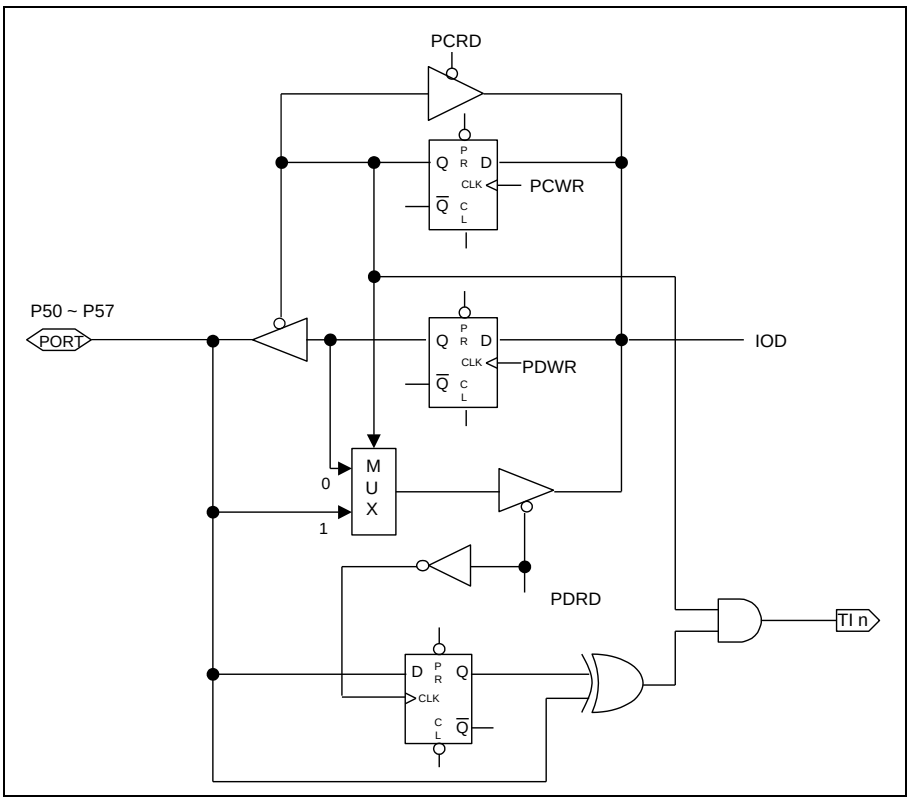
Note: Pull-high and Open-drain are not shown in the figure.

Figure 7-6 I/O Port and I/O Control Register Circuit for Port 6 and Port 7



Note: Pull-high and Open-drain are not shown in the figure.

Figure 7-7 I/O Port and I/O Control Register Circuit for P60 (/INT)



Note: Pull-high (down) and Open-drain are not shown in the figure.

Figure 7-8 I/O Port and I/O Control Register Circuit for Ports 50~57

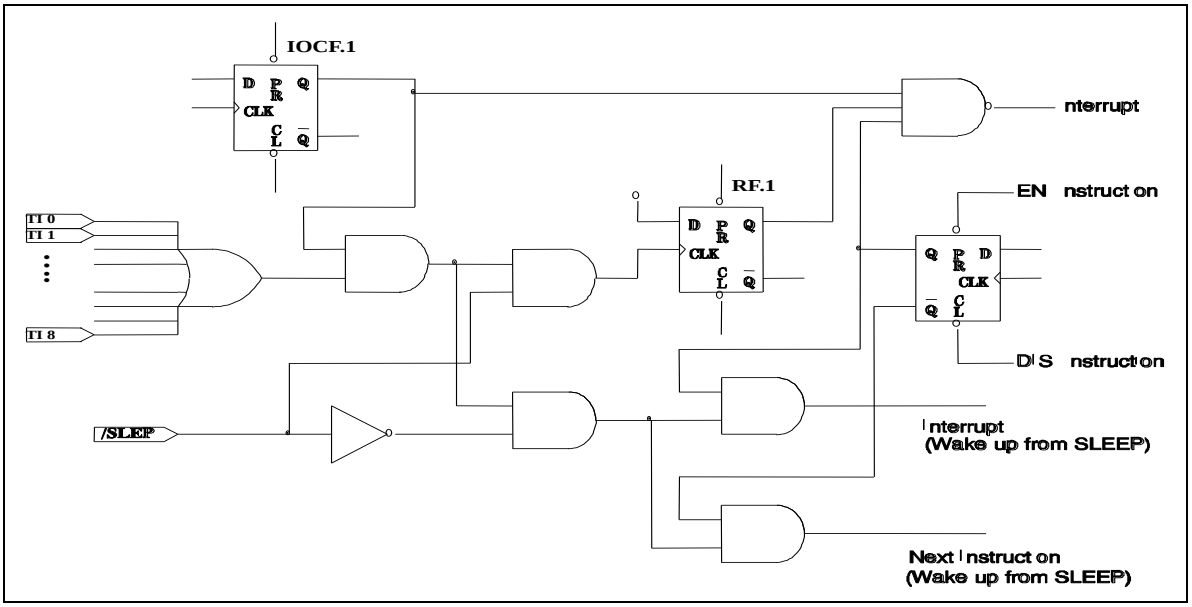


Figure 7-9 Port 5 Input Change Interrupt / Wake-up Block Diagram

7.4.1 Usage of Ports 5, 7 Input Change Wake-up/Interrupt Function

(1) Wake-up	(2) Wake-up and Interrupt
(a) Before Sleep	(a) Before Sleep
1. Disable WDT	1. Disable WDT
2-1. Read I/O Port 5 (MOV R5,R5)	2-1. Read I/O Port 5 (MOV R5,R5)
2-2. Read I/O Port 7 (MOV R7,R7)	2-2. Read I/O Port 7 (MOV R7,R7)
3. Execute "ENI" or "DISI"	3. Execute "ENI" or "DISI"
4. Enable wake-up bit (Set RE ICWE =1)	4. Enable wake-up bit (Set RE ICWE =1)
5. Execute "SLEP" instruction	5. Enable interrupt (Set IOCF ICIE =1)
(b) After wake-up	6. Execute "SLEP" instruction
→ Next instruction	(b) After wake-up
	1. IF "ENI" → Interrupt vector (008H)
	2. IF "DISI" → Next instruction
(3) Interrupt	
(a) Before Port 5,7 pin change	
1-1. Read I/O Port 5 (MOV R5,R5)	
1-2. Read I/O Port 7 (MOV R7,R7)	
2. Execute "ENI" or "DISI"	
3. Enable interrupt (Set IOCF ICIE =1)	
(b) After Port 5,7 pin changed (interrupt)	
1. IF "ENI" → Interrupt vector (006H)	
2. IF "DISI" → Next instruction	

7.5 Reset and Wake-up

7.5.1 Reset and Wake-up Operation

A reset is initiated by one of the following events:

1. Power-on reset
2. /RESET pin input "low"
3. WDT time-out (if enabled)

The device is kept in reset condition for a period of approximately 18ms[3] (except in LXT mode) after the reset is detected. When in LXT2 mode, the reset time is 500ms. Two choices (18ms[3] or 4.5ms[4]) are available for WDT-time out period. Once a reset occurs, the following functions are performed (the initial Address is 000h):

- The oscillator continues running, or will be started (if in sleep mode).
- The Program Counter (R2) is set to all "0".

[3] VDD=5V, Setup time period = 16.5ms ± 30%
VDD=3V, Setup time period = 18ms ± 30%

[4] VDD=5V, Setup time period = 4.2ms ± 30%
VDD=3V, Setup time period = 4.5ms ± 30%

- All I/O port pins are configured as input mode (high-impedance state)
- The Watchdog Timer and prescaler are cleared
- When power is switched on, the upper three bits of R3 is cleared
- The IOCB0 register bits are set to all "1"
- The IOCC0 register bits are set to all "0"
- The IOCD0 register bits are set to all "1"
- Bits 7, 5, and 4 of the IOCE0 register are cleared
- Bits 5 and 4 of the RE register are cleared
- RF and IOCF0 registers are cleared

Executing the “SLEP” instruction will assert the sleep (power down) mode (When IDLE=“0”.). While entering into sleep mode, the Oscillator, TCC, TMR1 and TMR2 are stopped. The WDT (if enabled) is cleared but keeps on running.

During AD conversion, when “SLEP” instruction is set; the Oscillator, TMR1 and TMR2 keep on running. The WDT (if enabled) is cleared but keeps on running.

The controller can be awakened by:

Case 1 External reset input on /RESET pin

Case 2 WDT time-out (if enabled)

Case 3 Port 5, P70, P71 input status changes (if ICWE is enabled)

Case 4 AD conversion completed (if ADWE is enabled)

The first two cases (1 and 2) will cause the EM78P302N to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up). Cases 3 and 4 are considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) determines whether or not the controller branches to the interrupt vector following wake-up. If ENI is executed before SLEP, the instruction will begin to execute from Address 0x06 (Case 3) and 0x0C (Case 4) after wake-up. If DISI is executed before SLEP, the execution will restart from the instruction next to SLEP after wake-up.

Only one of Cases 2 to 4 can be enabled before entering into sleep mode. That is**:**

Case [a] If WDT is enabled before SLEP, all of the RE bit is disabled. Hence, the EM78P302N can be awakened only with Case 1 or Case 2. Refer to the section on Interrupt (Section 7.6) for further details.

Case [b] If Port 5, P70, P71 Input Status Change is used to wake up the EM78P302N and the ICWE bit of the RE register is enabled before SLEP, and WDT must be disabled. Hence, the EM78P302Ncan be awakened only with Case 3. Wake-up time is dependent on the oscillator mode. In RC mode, Wake-up time is 10μs (for stable oscillators). In HXT2 (4 MHz) mode, Wake-up time is 800μs (for stable oscillators), and in LXT2 mode, Wake-up time is 2 ~ 3s.

Case [c] If completed AD conversion is used to wake-up the EM78P302N and ADWE bit of RE register is enabled before SLEP, WDT must be disabled by software. Hence, the EM78P302N can be awakened only with Case 4.

If Port 5, P70, P71 Input Status Change Interrupt is used to wake up the EM78P302N (as in Case [b] above), the following instructions must be executed before SLEP:

```
BC              R3, 6              ; Select Segment 0
MOV             A, @00xx1110b      ; Select WDT prescaler and Disable WDT
IOW             IOCE0
WDTC                               ; Clear WDT and prescaler
MOV             R5, R5             ; Read Port 5
MOV             R7, R7             ; Read Port 7
ENI (or DISI)                      ; Enable (or disable) global interrupt
MOV             A, @xxxxxx1xb      ; Enable Port 5,7 input change wake-up bit
MOV             RE, A
MOV             A, @1xxxxx1xb      ; Enable Port 5,7 input change interrupt
IOW             IOCF0
SLEP                               ; Sleep
```

7.5.2 Wake-up and Interrupt Modes Operation Summary

The controller can be awakened from sleep mode and idle mode. The wake-up signals are listed as follows.

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
External INT	EXWE = 0, EXIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	EXWE = 0, EXIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	EXWE = 1, EXIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	EXWE = 1, EXIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
Port 5, P70, P71 pin change	ICWE = 0, ICIE = 0, P7ICIE = 0	Wake-up is invalid		Wake-up is invalid.		Interrupt is invalid		Interrupt is invalid	
	ICWE = 0, ICIE = 1, P7ICIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	ICWE = 1, ICIE = 0, P7ICIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	ICWE = 1, ICIE = 1, P7ICIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
TCC Overflow	TCIE = 0	Wake-up is invalid		wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	TCIE = 1			Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
AD Conversion Complete	ADWE = 0, ADIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	ADWE = 0, ADIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	ADWE = 1, ADIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	ADWE = 1, ADIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
PWM1 period match interrupt	PWM1IE = 0	Wake-up is invalid		wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	PWM1IE = 1			Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
PWM2 period match interrupt	PWM2IE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	PWM2IE = 1			Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
PWM1 duty match interrupt	DT1IE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	DT1IE = 1			Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
PWM2 duty match interrupt	DT2IE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	DT2IE = 1			Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
WDT Timeout	WDTE = 1	Wake up + Reset		Wake up + Reset		Reset		Reset	
Low Voltage Reset		Wake up + Reset		Wake up + Reset		Reset		Reset	

7.5.3 Register Initial Values after Reset

The following summarizes the initialized values for registers.

Legend: ***"x"*** *= not used* ***"P"*** *= previous value before reset*
"u" *= unknown or don't care* ***"t"*** *= check "Reset Type" Table in Section 7.5.5*

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC50	Bit Name	C57	C56	C55	C54	C53	C52	C51	C50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC60	Bit Name	C67	×	×	×	×	×	×	C60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC70	Bit Name	×	×	×	×	×	×	C71	C70
		Power-on	0	0	0	0	0	0	1	1
		/RESET and WDT	0	0	0	0	0	0	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC90 (TMR1)	Bit Name	TMR1[7]	TMR1[6]	TMR1[5]	TMR1[4]	TMR1[3]	TMR1[2]	TMR1[1]	TMR1[0]
		Power-on	0	0	0	0	0	0	0	1
		/RESET and WDT	0	0	0	0	0	0	0	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCA0 (TMR2)	Bit Name	TMR2[7]	TMR2[6]	TMR2[5]	TMR2[4]	TMR2[3]	TMR2[2]	TMR2[1]	TMR2[0]
		Power-on	0	0	0	0	0	0	0	1
		/RESET and WDT	0	0	0	0	0	0	0	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCB0 (PDCR)	Bit Name	/PD57	/PD56	/PD55	/PD54	/PD53	/PD52	/PD51	/PD50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCC0 (ODCR)	Bit Name	OD67	×	×	×	×	×	×	OD60
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCD0 (PHCR1)	Bit Name	/PH57	/PH56	/PH55	/PH54	/PH53	/PH52	/PH51	/PH50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCE0	Bit Name	WDTE	EIS	ADIE	×	PSWE	PSW2	PSW1	PSW0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCF0	Bit Name	P7ICIE	DT2IE	DT1IE	PWM2IE	PWM1IE	EXIE	ICIE	TCIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC51 (HSCR1)	Bit Name	HS57	HS56	HS55	HS54	HS53	HS52	HS51	HS560
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC61 (HSCR2)	Bit Name	HS67	×	×	×	×	×	×	HS60
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC71 (HDCR1)	Bit Name	HD57	HD56	HD55	HD54	HD53	HD52	HD51	HD50
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC81 (HDCR2)	Bit Name	HD67	×	×	×	×	×	×	HD60
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC91 (DeadTCR)	Bit Name	IPWM2A	IPWM1A	PWM2A	PWM1A	DEADT2E	DEADT1E	×	×
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCA1 (DeadTR)	Bit Name	×	×	×	×	DEADTR3	DEADTR2	DEADTR1	DEADTR0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCB1	Bit Name	×	×	×	×	×	×	×	/PH70
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	1	1	1	1	1	1	1	P
N/A	IOCF1 (PHCR2)	Bit Name	/PH67	×	×	×	×	×	×	/PH60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	CONT	Bit Name	INTE	INT	TS	TE	PSTE	PST2	PST1	PST0
		Power-on	1	0	1	1	0	0	0	0
		/RESET and WDT	1	0	1	1	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×00	R0 (IAR)	Bit Name	–	–	–	–	–	–	–	–
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×01	R1 (TCC)	Bit Name	–	–	–	–	–	–	–	–
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×02	R2 (PC)	Bit Name	–	–	–	–	–	–	–	–
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	Jump to Address 0x06 or continue to execute next instruction							
0×03	R3 (SR)	Bit Name	RST	IOCS	–	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	t	t	P	P	P
		Wake-up from Pin Change	1	P	P	t	t	P	P	P
0×04	R4 (RSR)	Bit Name	SBANK	BS0	–	–	–	–	–	–
		Power-on	0	0	U	U	U	U	U	U
		/RESET and WDT	0	0	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×05	R5	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×06	R6	Bit Name	P67	×	×	×	×	×	×	P60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×07	R7	Bit Name	×	×	×	×	×	×	P71	P70
		Power-on	0	0	0	0	0	0	1	1
		/RESET and WDT	0	0	0	0	0	0	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×08	R8 (AISR)	Bit Name	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×09	R9 (ADCON)	Bit Name	VREFS	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0A	RA (ADOC)	Bit Name	CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	VREF1	VREF0	ADICS
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×0B	RB (ADDATA)	Bit Name	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	U	U	U	U	U	U	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0C	RC (ADDATA1H)	Bit Name	×	×	×	×	AD11	AD10	AD9	AD8
		Power-on	0	0	0	0	U	U	U	U
		/RESET and WDT	0	0	0	0	U	U	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0D	RD (ADDATA1L)	Bit Name	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	U	U	U	U	U	U	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0E	RE (ISR2)	Bit Name	×	×	ADIF	×	ADWE	×	ICWE	×
		Power-on	1	0	0	0	0	0	0	0
		/RESET and WDT	1	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0F	RF (ISR1)	Bit Name	P7ICIF	DT2IF	DT1IF	PWM2IF	PWM1IF	EXIF	ICIF	TCIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×05	Bank 1 R5	Bit Name	MLB	TRS	×	×	×	RBit10	RBit9	RBit8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×06	BANK1 R6	Bit Name	RBit7	RBit6	RBit5	RBit4	RBit3	RBit2	RBit1	RBit0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×07	BANK1 R7 (PWMCON)	Bit Name	IPWM2E	IPWM1E	×	×	×	PWMCAS	PWM2E	PWM1E
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×08	BANK1 R8 (TMRCON)	Bit Name	T2EN	T1EN	T2P2	T2P1	T2P0	T1P2	T1P1	T1P0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×09	BANK1 R9 (PRD1)	Bit Name	PWM1[7]	PWM1[6]	PWM1[5]	PWM1[4]	PWM1[3]	PWM1[2]	PWM1[1]	PWM1[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0A	BANK1 RA (PRD2)	Bit Name	PWM2[7]	PWM2[6]	PWM2[5]	PWM2[4]	PWM2[3]	PWM2[2]	PWM2[1]	PWM2[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0B	BANK1 RB (DT1)	Bit Name	DT1[7]	DT1[6]	DT1[5]	DT1[4]	DT1[3]	DT1[2]	DT1[1]	DT1[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0C	BANK1 RC (DT2)	Bit Name	DT2[7]	DT2[6]	DT2[5]	DT2[4]	DT2[3]	DT2[2]	DT2[1]	DT2[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0E	Bank 1 RE	Bit Name	×	×	×	×	×	×	×	EXWE
		Power-on	0	0	1	1	0	0	0	0
		/RESET and WDT	0	0	1	1	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0F	Bank 1 RF	Bit Name	-	TIMERSC	CPUS	IDLE	SHS1	SHS0	RCM1	RCM0
		Power-on	0	1	1	0	1	1	WORD1 <6~5>	
		/RESET and WDT	0	1	1	0	1	1	WORD1 <6~5>	
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x10~0x3F	R10~R3F	Bit Name	–	–	–	–	–	–	–	–
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

7.5.4 Controller Reset Block Diagram

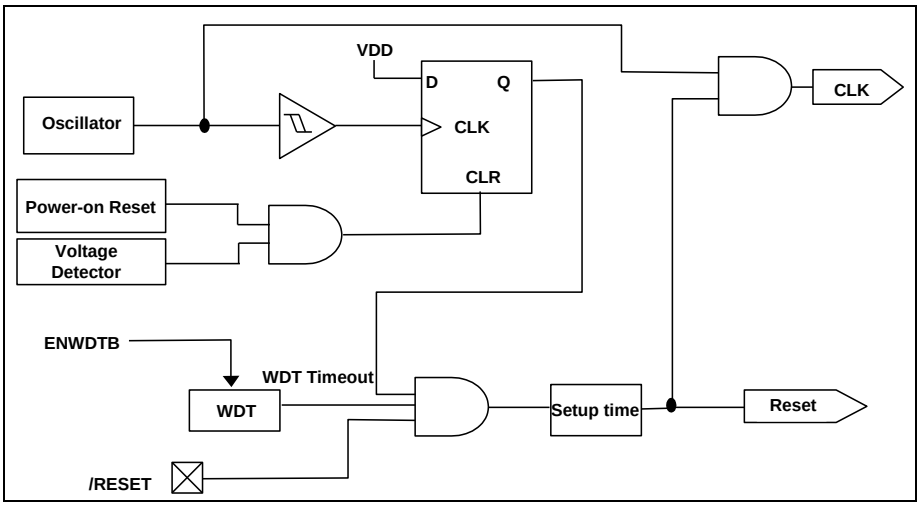


Figure 7-10 Controller Reset Block Diagram

7.5.5 The T and P Status under Status Register

A reset condition is initiated by one of the following events:

1. Power-on reset
2. /RESET pin input "low"
3. WDT time-out (if enabled)

The values of T and P as listed in the table below, are used to check how the processor wakes up.

Reset Type	RST	T	P
Power-on	0	1	1
/RESET during Operating mode	0	*P	*P
/RESET wake-up during Sleep mode	0	1	0
LVR during Operating mode	0	*P	*P
LVR wake-up during Sleep mode	0	1	0
WDT during Operating mode	0	0	1
WDT wake-up during Sleep mode	0	0	0
Wake-up on pin change during Sleep mode	1	1	0

*P: Previous status before reset

The following shows the events that may affect the status of T and P.

Event	RST	T	P
Power-on	0	1	1
WDTC instruction	*P	1	1
WDT time-out	0	0	*P
SLEP instruction	*P	1	0
Wake-up on pin changed during Sleep mode	1	1	0

*P: Previous value before reset

7.6 Interrupt

The EM78P302N has five interrupts enumerated below**:**

1. PWM1~2 period match and duty cycle match interrupt
2. Port 5, P70, P71 Input Status Change Interrupt
3. External interrupt [(P60, /INT) pin]
4. Analog to Digital conversion completed
5. PWM1, 2 underflow interrupt

Before the Port 5, P70, P71 Input Status Change Interrupt is enabled, reading Port 5, P70, P71 (e.g. "MOV R5, R5" and "MOV R7, R7") is necessary. Each Port 5, P70, P71 pin will have this feature if its status changes. The Port 5, P70, P71 Input Status Change Interrupt will wake up the EM78P302N from sleep mode if it is enabled prior to going into sleep mode by executing SLEP instruction. When wake up occurs, the controller will continue to execute program in-line if the global interrupt is disabled. If enabled, the global interrupt will branch out to the Interrupt Vector 006H.

External interrupt equipped with digital noise rejection circuit (input pulse less than system clock time is eliminated as noise). However, under Low Crystal oscillator (LXT) mode the noise rejection circuit will be disabled. Edge selection is possible with INTE of CONT. When an interrupt is generated by the External interrupt (when enabled), the next instruction will be fetched from Address 003H. Refer to Word 1 Bits 9 and 8, Section 7.13.2, *Code Option Register (Word 1)* for digital noise rejection definition.

RF and RE are the interrupt status register that records the interrupt requests in the relative flags/bits. IOCF0 and IOCE0 are Interrupt mask registers. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Once in the interrupt service routine, the source of an interrupt can be determined by polling the flag bits in RF. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine to avoid recursive interrupts.

When interrupt mask bit is “Enabled”, the flag in the Interrupt Status Register (RF) is set regardless of the ENI execution. Note that the result of RF will be the Logic AND of RF and IOCF0 (refer to figure below). The RETI instruction ends the interrupt routine and enables the global interrupt (the ENI execution).

When an interrupt is generated by the Timer clock/counter (when enabled), the next instruction will be fetched from Address 009, 012, 015, 018 and 01BH (TCC, PWM1~2 periods match and duty match respectively).

When an interrupt generated by AD conversion is completed (when enabled), the next instruction will be fetched from Address 00CH.

Before an interrupt subroutine is executed, the contents of ACC and the R3 and R4 registers are saved first by the hardware. If another interrupt occurs, the ACC, R3, and R4 will be replaced by the new interrupt. After an interrupt service routine is completed, the ACC, R3, and R4 registers are restored.

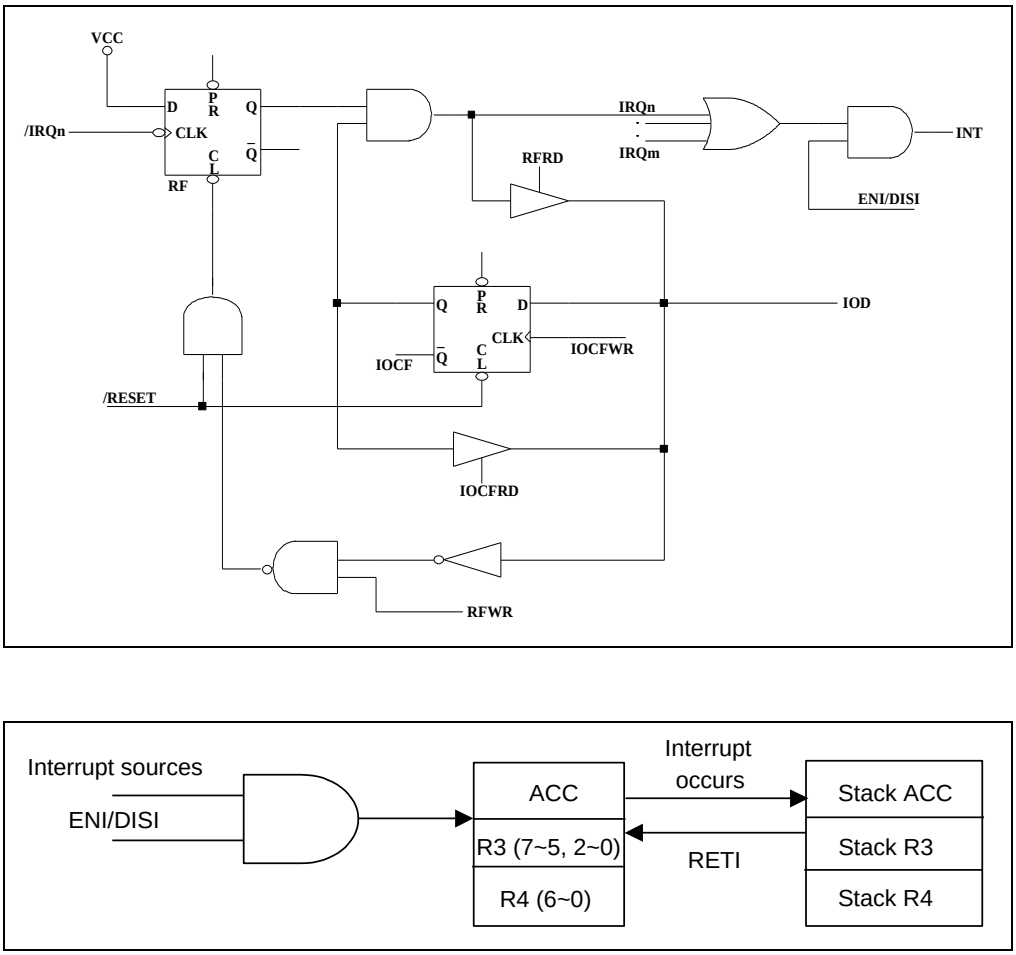


Figure 7-11 Interrupt Back-up Diagram

In EM78P302N, each individual interrupt source has its own interrupt vector as depicted in the table below.

Interrupt Vector	Interrupt Status	Priority *
003H	External interrupt	1
006H	Port 5, P70, P71 pin change	2
009H	TCC overflow interrupt	3
00CH	AD conversion complete interrupt	4
012H	PWM1 period match interrupt	5
015H	PWM2 period match interrupt	6
018H	PWM1 duty match interrupt	7
01BH	PWM2 duty match interrupt	8

Note: **Priority: 1 = highest ; 8 = lowest priority*

7.7 Analog-to-Digital Converter (ADC)

The analog-to-digital circuitry consists of an 8-bit analog multiplexer; three control registers (AISR/R8, ADCON/R9, and ADOC/RA), three data registers (ADDATA1/RB, ADDATA1H/RC, and ADDATA1L/RD) and an ADC with 12-bit resolution as shown in the functional block diagram below. The analog reference voltage (Vref) and the analog ground are connected via separate input pins. Connecting to an external VREF is more accurate than connecting to an internal VDD.

The ADC module utilizes successive approximation to convert the unknown analog signal into a digital value. The result is fed to the ADDATA, ADDATA1H, and ADDATA1L. Input channels are selected by the analog input multiplexer via the ADCON register Bits ADIS1 and ADIS0.

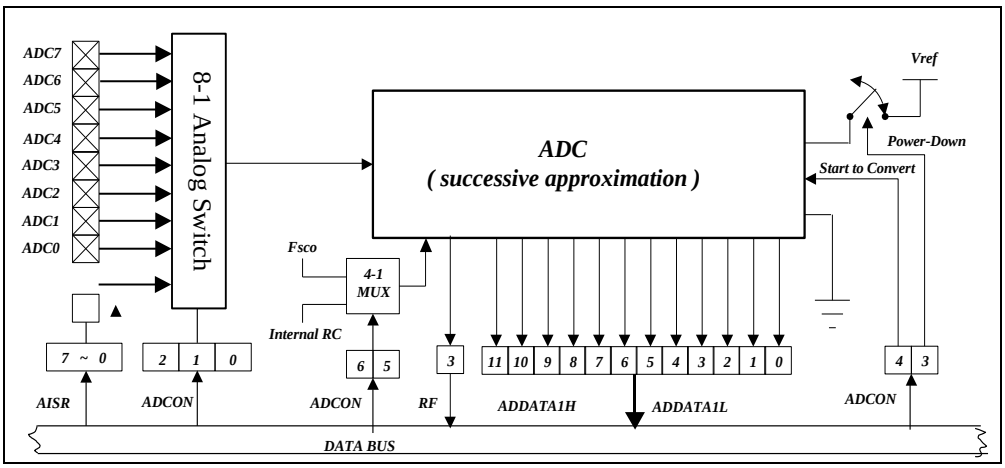


Figure 7-12 Analog-to-Digital Conversion Functional Block Diagram

7.7.1 ADC Control Register (AISR/R8, ADCON/R9, ADOC/RA)

7.7.1.1 R8 (AISR: ADC Input Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0

The **AISR** register individually defines the P5, P6 and P7 pins as analog inputs or as digital I/O.

Bit 7 (ADE7): AD converter enable bit of P57 pin

0 : Disable ADC7, P57 functions as I/O pin

1 : Enable ADC7 to function as analog input pin

Bit 6 (ADE6): AD converter enable bit of P55 pin

0 : Disable ADC6, P55 functions as I/O pin

1 : Enable ADC6 to function as analog input pin

Bit 5 (ADE5): AD converter enable bit of P70 pin

0 : Disable ADC5, P70 functions as I/O pin

1 : Enable ADC5 to function as analog input pin

Bit 4 (ADE4): **When ADPINOPT=0:**

AD converter enable bit of P54 pin

0 : Disable ADC4, P54 functions as I/O pin

1 : Enable ADC4 to function as analog input pin

When ADPINOPT=1:

AD converter enable bit of P67 pin

0 : Disable ADC4, P67 functions as I/O pin

1 : Enable ADC4 to function as analog input pin

Bit 3 (ADE3): AD converter enable bit of P53 pin

0 : Disable ADC3, P53 functions as I/O pin

1 : Enable ADC3 to function as analog input pin

Bit 2 (ADE2): AD converter enable bit of P52 pin

0 : Disable ADC2, P52 functions as I/O pin

1 : Enable ADC2 to function as analog input pin

Bit 1 (ADE1): AD converter enable bit of P51 pin

0 : Disable ADC1, P51 acts as I/O pin

1 : Enable ADC1 acts as analog input pin

Bit 0 (ADE0): AD converter enable bit of P50 pin

0 : Disable ADC0, P50 functions as I/O pin

1 : Enable ADC0 to function as analog input pin

7.7.1.2 R9 (ADCON: ADC Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VREFS	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0

The **ADCON** register controls the operation of the AD conversion and decides which pin should be currently active.

Bit 7 (VREFS): The input source of Vref of the ADC

0 : The Vref of the ADC is connected to internal reference voltage (default value), and the P54/TCC/VREF/(ADPINOPT=0:ADC4) pin carries out the function of P54.

1 : The Vref of the ADC is connected to P54/TCC/VREF/ (ADPINOPT=0: ADC4)

NOTE

- *The P54/TCC/VREF/(ADPINOPT=0:ADC4) pin cannot be applied to TCC, ADC4 and VREF at the same time. If P54/TCC/VREF/(ADPINOPT=0:ADC4) functions as VREF analog input pin, then CONT Bit 5 "TS" must be "0."*
- *The P54/TCC/VREF/(ADPINOPT=0:ADC4) Pin Priority is as follows:*

P54/TCC/ADC4/VREF Pin Priority		
High	**Medium**	**Low**
VREF/ADC4	**TCC**	**P54**

Bit 6 ~ Bit 5 (CKR1 ~ CKR0): The prescaler of ADC oscillator clock rate

CPUS	CKR1 : CKR0	Operation Mode	Max. Operation Freq. (if TAD=4μs, matches 372N)	Max. Operation Freq. (if TAD=1μs, matches 372N)
1	00 (default)	$F_{OSC}/16$	4 MHz	16 MHz
1	01	$F_{OSC}/4$	1 MHz	4 MHz
1	10	$F_{OSC}/64$	16 MHz	-
1	11	$F_{OSC}/1$	-	1 MHz
0	××		16K/128kHz	16K/128kHz

Bit 4 (ADRUN): ADC starts to RUN

0: Reset upon completion of the conversion. This bit **cannot** be reset though software.

1: AD conversion is started. This bit can be set by software.

Bit 3 (ADPD): ADC Power-down mode

0: Switch off the resistor reference to conserve power even while the CPU is operating

1: ADC is operating

Bits 2 ~ 0 (ADIS2 ~ ADIS0): Analog Input Select

ADICS	ADIS2	ADIS1	ADIS0	Analog Input Select
0	0	0	0	ADIN0/P50
0	0	0	1	ADIN1/P51
0	0	1	0	ADIN2/P52
0	0	1	1	ADIN3/P53
0	1	0	0	ADIN4 / (ADPINOPT=0:P54) or (ADPINOPT=1:P67)
0	1	0	1	ADIN5/P70
0	1	1	0	ADIN6/P55
0	1	1	1	ADIN7/P57
1	1	0	0	Internal ADC Channel Select: 1/4 VDD
1	1	0	1	Internal ADC Channel Select: 1/2 VDD
1	1	1	0	Reserved
1	1	1	1	Reserved

7.7.1.3 RA (ADOC: AD Offset Calibration Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	VREF1	VREF0	ADICS

Bit 7 (CALI): Calibration enable bit for ADC offset

0 = Disable the Calibration

1 = Enable the Calibration

Bit 6 (SIGN): Polarity bit of offset voltage

0 = Negative voltage

1 = Positive voltage

Bit 5 ~ Bit 3 (VOF[2] ~ VOF[0]): Offset voltage bits

VOF[2]	VOF[1]	VOF[0]	EM78P302N
0	0	0	0 LSB
0	0	1	2 LSB
0	1	0	4 LSB
0	1	1	6 LSB
1	0	0	8 LSB
1	0	1	10 LSB
1	1	0	12 LSB
1	1	1	14 LSB

Bits 2 ~ 1 (VREF1~0): ADC internal reference voltage source.

VREFSEL in Option Word 3 bit 11	VREF1	VREF0	ADC Int. Ref. Volt.
0	0	0	VDD
0	0	1	4.0V ± 1%
0	1	0	3.0V ± 1%
0	1	1	2.5V ± 1%
1	0	0	VDD
1	0	1	4.0V ± 1%
1	1	0	3.0V ± 1%
1	1	1	2.0V ± 1%

Bit 0 (ADICS): ADC internal channel select**.** (Select ADC internal 1/4 VDD or 1/2 VDD output pin connects to ADC input)

0 = Disable

1 = Enable

7.7.1.4 Bank 1 RF (IRC Switch Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	TIMERSC	CPUS	IDLE	SHS1	SHS0	RCM1	RCM0

Bits 3 ~ 2 (SHS1~0): Select AD sample and Hold period

SHS1	SHS0	AD Sample and Hold Period (TAD)
0	0	2
0	1	4
1	0	8
1	1	12 (default)

7.7.2 ADC Data Register (ADDATA/RB, ADDATA1H/RC, ADDATA1L/RD)

When AD conversion is completed, the result is loaded to the ADDATA, ADDATA1H and ADDATA1L registers. The ADRUN bit is cleared, and the ADIF is set.

7.7.3 ADC Sampling Time

The accuracy, linearity, and speed of the successive approximation of the AD converter are dependent on the properties of the ADC and the comparator. The source impedance and the internal sampling impedance directly affect the time required to charge the sample holding capacitor. The application program controls the length of the sample time to meet the specified accuracy. Generally speaking, the program should wait for 2μs for each KΩ of the analog source impedance and at least 2μs for the low-impedance source. The maximum recommended impedance for analog source is 10KΩ at Vdd=5V. After the analog input channel is selected, this acquisition time must be done before the conversion is started.

7.7.4 AD Conversion Time

CKR1 and CKR0 select the conversion time, in terms of instruction cycles (TAD). This allows the MCU to run at the maximum frequency without sacrificing the AD conversion accuracy. For the EM78P302N, the conversion time per bit is about 1μs. The table below shows the relationship between TAD and the maximum operating frequencies.

TAD = 1μs

CPUS	CKR1 : CKR0	Operation Mode	Max. Operation Frequency	Max. Conversion Rate/Bit	Max. Conversion Rate
1	00 (default)	F_{OSC}/16	16 MHz	1 MHz (1μs)	16*1μs=16μs (62.5kHz)
1	01	F_{OSC}/4	4 MHz	1 MHz (1μs)	16*1μs=16μs (62.5kHz)
1	10	F_{OSC}/64	-	-	-
1	11	F_{OSC}/1	1 MHz	1 MHz (1μs)	16*1μs=16μs (62.5kHz)
0	××	-	16K/128kHz	-	-

TAD = 4μs

CPUS	CKR1 : CKR0	Operation Mode	Max. Operation Frequency	Max. Conversion Rate/Bit	Max. Conversion Rate
1	00 (default)	F_{OSC}/16	4 MHz	250kHz (4μs)	16*4μs=64μs (15.625kHz)
1	01	F_{OSC}/4	1 MHz	250kHz (4μs)	16*4μs=64μs (15.625kHz)
1	10	F_{OSC}/64	16 MHz	250kHz (4μs)	16*4μs=64μs (15.625kHz)
1	11	F_{OSC}/1	-	-	-
0	××	-	16K/128kHz	-	-

NOTE

- *Pin not used as an analog input pin can be used as regular input or output pin.*
- *During conversion, do not perform output instruction to maintain precision for all of the pins.*

7.7.5 ADC Operation during Sleep Mode

In order to obtain a more accurate ADC value and reduce power consumption, the AD conversion remains operational during sleep mode. As the SLEP instruction is executed, all the MCU operations will stop except for the Oscillator, TCC, and AD conversion.

The AD Conversion is considered completed as determined by**:**

1. The ADRUN bit of the R9 register is cleared to “0”.
2. The ADIF bit of the RE register is set to “1”.
3. The ADWE bit of the RE register is set to “1”. Wakes up from ADC conversion (where it remains in operation during sleep mode).
4. Wake up and execution of the next instruction if the ADIE bit of the IOCE0 is enabled and the “DISI” instruction is executed.
5. Wake up and enters into Interrupt vector (Address 0x00C) if the ADIE bit of the IOCE0 is enabled and the “ENI” instruction is executed.
6. Enters into an Interrupt vector (Address 0x00C) if the ADIE bit of the IOCE0 is enabled and the “ENI” instruction is executed.

The results are fed into the ADDATA, ADDATA1H, and ADDATA1L registers when the conversion is completed. If the ADIE is enabled, the device will wake up. Otherwise, the AD conversion will be shut off, no matter what the status of the ADPD bit is.

7.7.6 Programming Process/Considerations

7.7.6.1 Programming Process

Follow these steps to obtain data from the ADC**:**

1. Write to the eight bits (ADE7: ADE0) on the R8 (AISR) register to define the characteristics of R5 (digital I/O, analog channels, or voltage reference pin)
2. Write to the R9/ADCON register to configure the AD module**:**
   a) Select the ADC input channel (ADIS2 : ADIS0)
   b) Define the AD conversion clock rate (CKR1 : CKR0)
   c) Select the VREFS input source of the ADC
   d) Set the ADPD bit to 1 to begin sampling
3. Set the ADWE bit, if the wake-up function is employed

4. Set the ADIE bit, if the interrupt function is employed
5. Write “ENI” instruction, if the interrupt function is employed
6. Set the ADRUN bit to 1
7. Write “SLEP” instruction or Polling.
8. Wait for wake-up or for the ADRUN bit to be cleared to “0” , interrupt flag (ADIF) is set “1”, or ADC interrupt occurs.
9. Read the ADDATA or ADDATA1H and ADDATA1L conversion data registers. If the ADC input channel changes at this time, the ADDATA, ADDATA1H, and ADDATA1L values can be cleared to ‘0’.
10. Clear the interrupt flag bit (ADIF).
11. For next conversion, go to Step 1 or Step 2 as required. At least two TAD is required before the next acquisition starts.

NOTE

In order to obtain accurate values, it is necessary to avoid any data transition on the I/O pins during AD conversion

7.7.6.2 Sample Demo Programs

```
R_0 == 0          ; Indirect addressing register
PSW == 3          ; Status register
PORT5 == 5
PORT6 == 6
R_E== 0XE         ; Interrupt status register
```

B. Define a Control Register

```
IOC50 == 0X5      ; Control Register of Port 5
IOC60 == 0X6      ; Control Register of Port 6
IOCE0== 0XE       ; Interrupt Mask Register 2
C_INT== 0XF       ; Interrupt Mask Register
```

C. ADC Control Register

```
ADDATA == 0xB     ; The contents are the results of ADC
AISR == 0x08      ; ADC input select register
ADCON == 0x9      ;  7     6    5    4      3     2     1     0
                  ; VREFS CKR1 CKR0 ADRUN ADPD ADIS2 ADIS1 ADIS0
```

D. Define Bits in ADCON

```
ADRUN == 0x4      ; ADC is executed as the bit is set
ADPD == 0x3       ; Power Mode of ADC
```

E. Program Starts

```
ORG 0             ; Initial address
JMP INITIAL       ;

ORG 0x0C          ; Interrupt vector
JMP CLRRE
;
;(User program section)
;
CLRRE:
MOV A,RE
AND A, @0BXX0XXXXX  ; To clear the ADIF bit, "X" by application
MOV RE,A
BS ADCON, ADRUN     ; To start to execute the next AD conversion
                    ; if necessary
RETI
INITIAL:
MOV A,@0B00000001   ; To define P50 as an analog input
MOV AISR,A
MOV A,@0B00001000   ; To select P50 as an analog input channel, and
                    ; AD power on
MOV ADCON,A         ; To define P50 as an input pin and set the
                    ; clock rate at fosc/16
En_ADC:
MOV A, @0BXXXXXXX1  ; To define P50 as an input pin, and the others
                    ; are dependent on applications
IOW PORT5
```

```
MOV A, @0BXXXX1XXX  ; Enable the ADWE wake-up function of ADC, "X"
                    ; by application
MOV RE,A
MOV A, @0BXX1XXXXX  ; Enable the ADIE interrupt function of ADC,
                    ; "X" by application
IOW IOCE0
ENI                 ; Enable the interrupt function

BS ADCON, ADRUN     ; Start to run the ADC

; If the interrupt function is employed, the following three lines
may be ignored

;If Sleep:
SLEP
;
;(User program section)
;

or
;If Polling:
POLLING:
JBC ADCON, ADRUN    ; To check the ADRUN bit continuously;
JMP POLLING         ; ADRUN bit will be reset as the AD conversion
                    ; is completed
;
;(User program section)
```

7.8 Dual Sets of PWM (Pulse Width Modulation)

7.8.1 Overview

In PWM mode, PWM1 and PWM2 pins produce to 8-bit resolution PWM output (see. the functional block diagram below). A PWM output consists of a time period and a duty cycle, and it keeps the output high. The baud rate of PWM is the inverse of the time period. Figure 7-14 ~ Figure 7-24 (PWM Output Timing) depicts the relationships between a time period and a duty cycle.

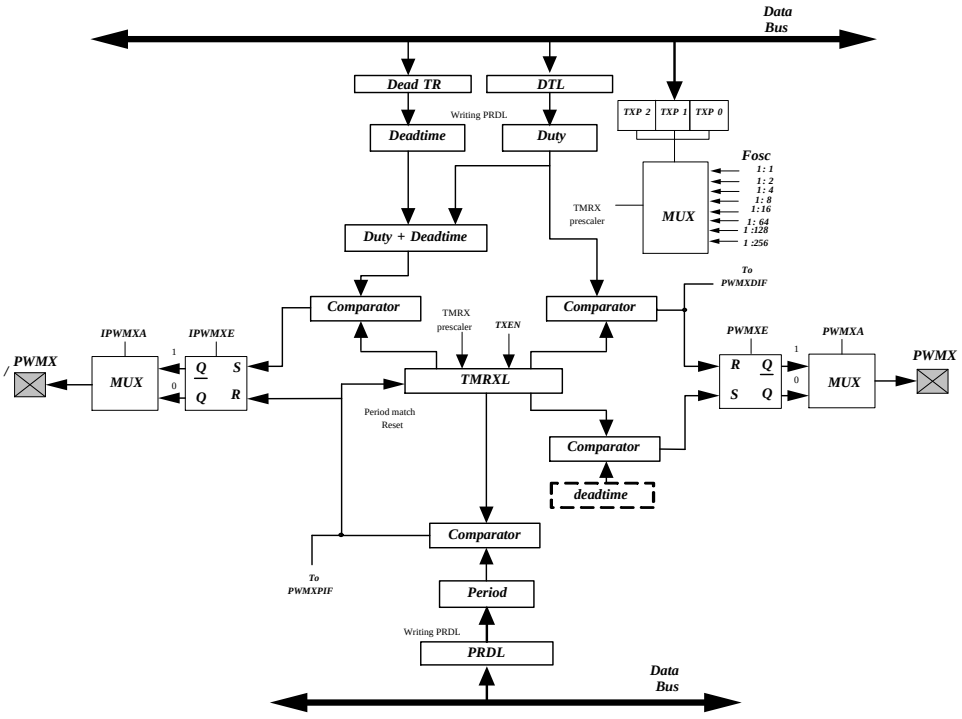


Figure 7-13 PWM System Block Diagram

PWM and /PWM (inverted PWM) can be used individually or used as dual PWM. When used individually, the definitions of active level between PWM and /PWM are somewhat different.

For example, set period and duty cycle (period > duty), PWMXE=1/0 and IPWMXE=0/1, PWMXA = 1/0, /PWMXA=1/0, and finally set TXEN = 1. The following figures show PWM output timing according to different PWMXA and /PWMXA settings.

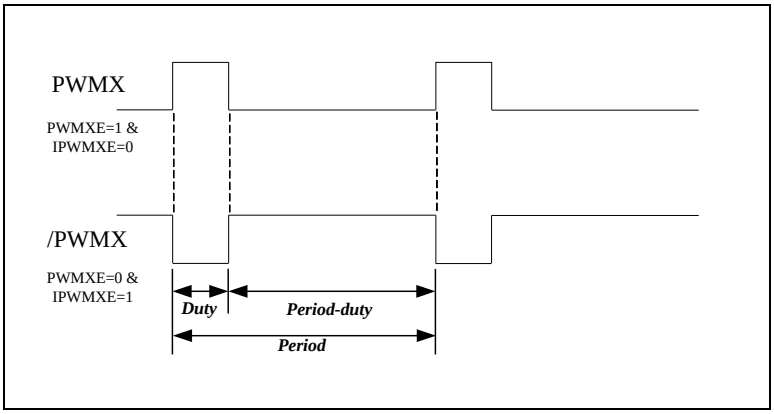


Figure 7-14 PWM Output Timing (PWMXA=0 and /PWMXA=0)

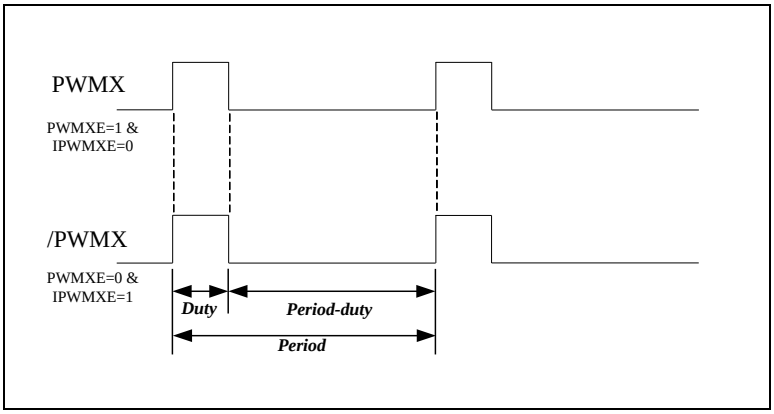


Figure 7-15 PWM Output Timing (PWMXA=0 and /PWMXA=1)

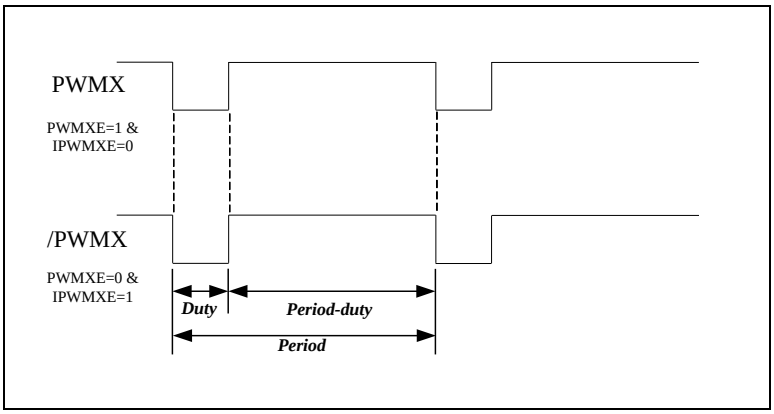


Figure 7-16 PWM Output Timing (PWMXA=1 and /PWMXA=0)

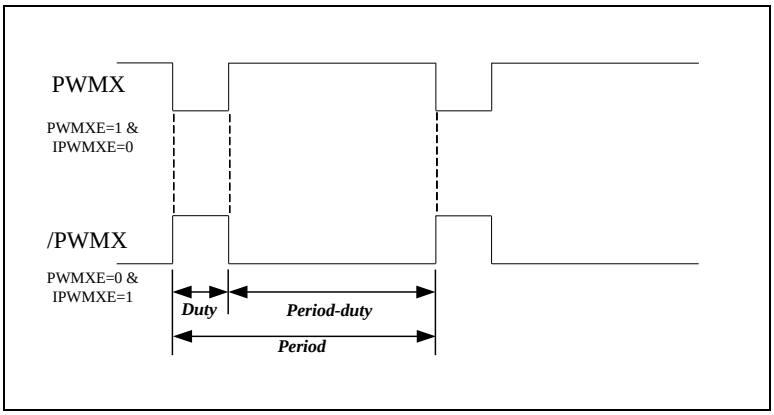


Figure 7-17 PWM Output Timing (PWMXA=1 and /PWMXA=1)

7.8.1.1 Dual PWM Function

It consists of a complementary PWM (i.e. PWMX and /PWMX), one outputs PWM signal and the other outputs inverted PWM signal, It can output any pulse width signal you want by programming the relative control registers.

The dead time mode is supported. It means that the complementary PWM signals can be controlled to get a time interval that the complementary PWM signals won't be intersected.

The following Figures 7-18 ~ 7-19 show the dual PWM output waveform.

Disable dead time control (DEADTXE = 0). Set period and duty cycle (period > duty). Set PWMXE & IPWMXE =1, PWMXA = 0/1, IPWMXA = 0/1, and finally set TXEN = 1.

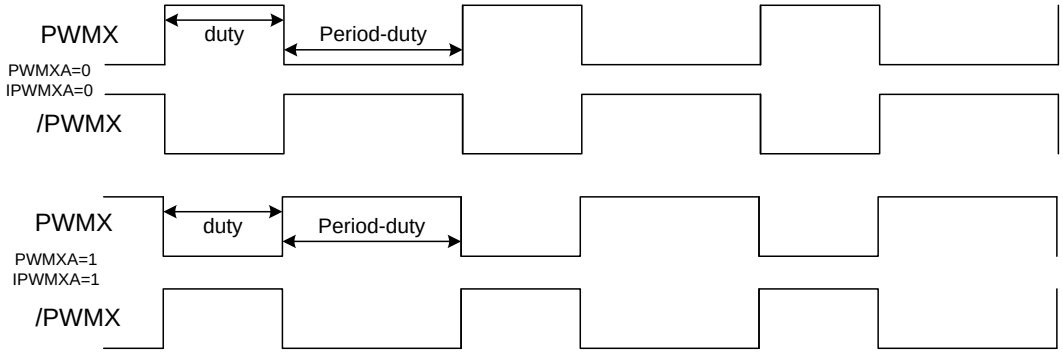


Figure 7-18 Dual PWMX Output Waveform (DEADTXE = 0)

Set dead time > 0 (set dead time prescaler if required). Enable dead time control (DEADTXE = 1). Set period and duty cycle (period > duty). Set PWMXE and IPWMXE =1, PWMXA = 0, IPWMXA = 0, and finally set TXEN = 1. For loading new duty, period, and dead time value at run time. Follow the "PWM Programming Process/Steps" descriptions.

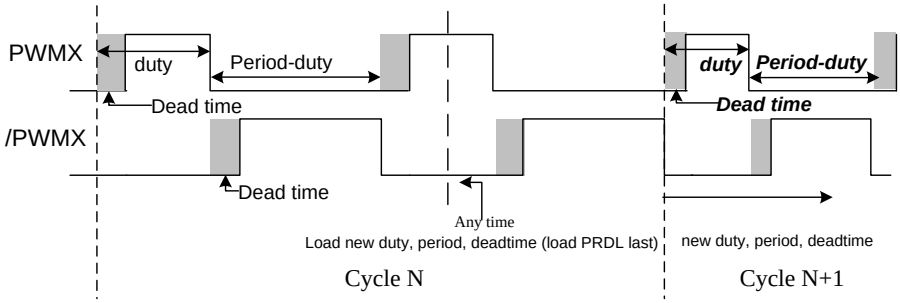


Figure 7-19 Dual PWMX Output Waveform (DEADTXE = 1, Dead Time > 0)

The following figures show PWM output timing according to different PWMXA and /PWMXA settings.

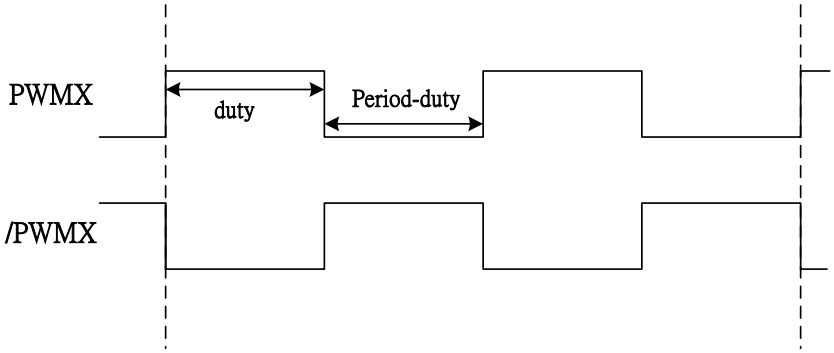


Figure 7-20 Dual PWMX Output Waveform (PWMXA = 0, IPWMXA=0, Dead Time = 0)

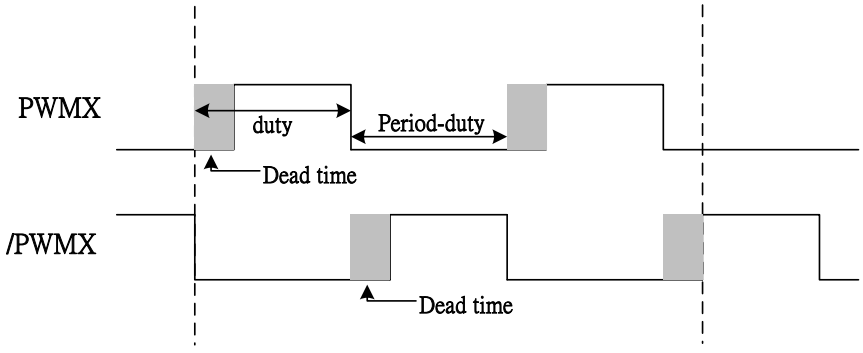


Figure 7-21 Dual PWMX Output Waveform (PWMXA = 0, IPWMXA=0, Dead Time > 0)

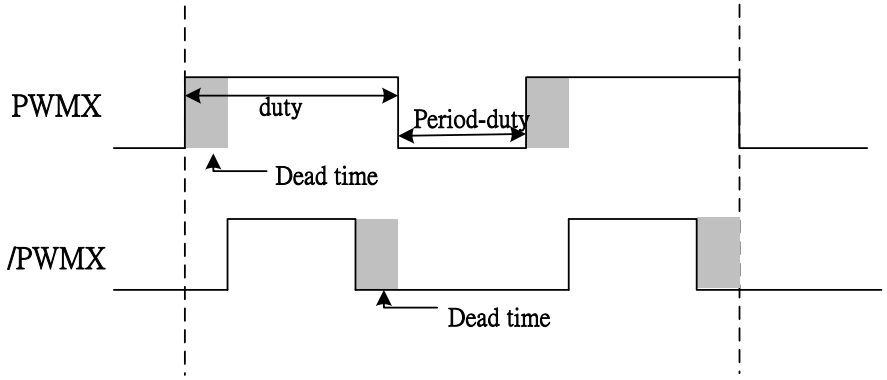


Figure 7-22 Dual PWMX Output Waveform (PWMXA = 1, IPWMXA=0, Dead Time > 0)

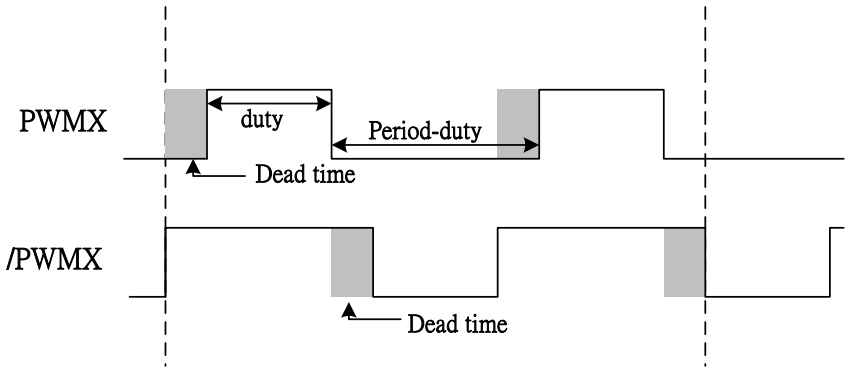


Figure 7-23 Dual PWMX Output Waveform (PWMXA = 0, IPWMXA=1, Dead Time > 0)

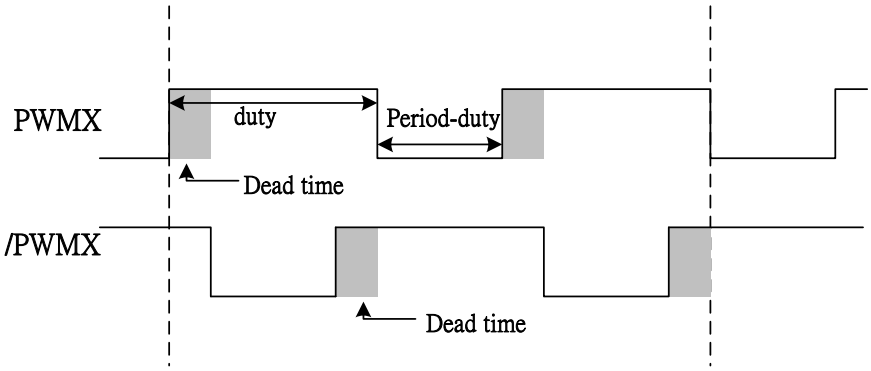


Figure 7-24 Dual PWMX Output Waveform (PWMXA = 1, IPWMXA=1, Dead Time > 0)

Note

The value in the dead-time register must be less than the value in the duty cycle register, in order to prevent unexpected behavior on both of the PWM outputs.

7.8.2 Increment Timer Counter (TMRX: TMR1 or TMR2)

TMRX are 8-bit clock counters with programmable prescalers. They are designed for the PWM module as baud rate clock generators. If employed, they can be turned off for power saving purposes by setting the T1EN bit [BANK1-R8<6>] or T2EN bit [BANK1-R8<7>] to "**0**".

TMR1 and TMR2 are internal designs and can be read only.

7.8.3 PWM Time Period (TMRX: TMR1 or TMR2)

PWM Time Period (PRDX: PRD1 or PRD2) The PWM time period is defined by writing to the PRDX register. When TMRX is equal to PRDX, the following events occur on the next increment cycle:

1) TMR is cleared
2) The PWMX is set to "**1**"
3) The PWM duty cycle is latched from DT1/DT2 to DL1/DL2

NOTE

*The PWM output will not be set, if the duty cycle is "**0**".*

4) The PWMXIF pin is set to "**1**"

The following formula describes how to calculate the PWM time period:

$$Period = (PRDX + 1) \times \left(\frac{1}{FOSC}\right) \times (TMRX \ \ prescale\ value)$$

Example:

PRDX=49; Fosc=4 MHz; TMRX (0, 0, 0) = 1:1,

then $Period = (49+1) \times \left(\frac{1}{4M}\right) \times 1 = 12.5\ \mu s$

7.8.4 PWM Duty Cycle (DTX: DT1 or DT2; DLX: DL1 or DL2)

The PWM duty cycle is defined by writing to the DTX register, and is latched from DTX to DLX while TMRX is cleared. When DLX is equal to TMRX, the PWMX pin is cleared. DTX can be loaded anytime. However, it cannot be latched into DLX until the current value of DLX is equal to TMRX.

The following formula describes how to calculate the PWM duty cycle:

$$Duty\ \ Cycle = (DTX) \times \left(\frac{1}{F_{OSC}}\right) \times (TMRX \ \ prescale\ \ value)$$

Example:

```
DTX=10; Fosc=4 MHz; TMRX (0, 0, 0) = 1:1,
```

then $Duty\ Cycle = 10 \times \left(\frac{1}{4M}\right) \times 1 = 2.5\mu s$

7.8.5 Comparator X

Changing the output status while a match occurs will simultaneously set the PWMXIF (TMRXIF) flag.

7.8.6 PWM Programming Process/Steps

Load PRDX with the PWM time period.

1. Load DTX with the PWM Duty Cycle.
2. Enable interrupt function by writing IOCF0, if required.
3. Set PWMX pin to be output by writing a desired value to BANK1-R7.
4. Load a desired value to Bank 1-R8 with TMRX prescaler value and enable both PWMx and TMRX

7.9 Timer

7.9.1 Overview

Timer 1 (TMR1) and Timer 2 (TMR2) (TMRX) are 8-bit clock counters with programmable prescalers. They are designed for the PWM module as baud rate clock generators. TMRX can be read only. The Timer 1 and Timer 2 will stop running when sleep mode occurs with AD conversion not running. However, if AD conversion is running when sleep mode occurs, Timer 1 and Timer 2 will keep on running.

7.9.2 Function Description

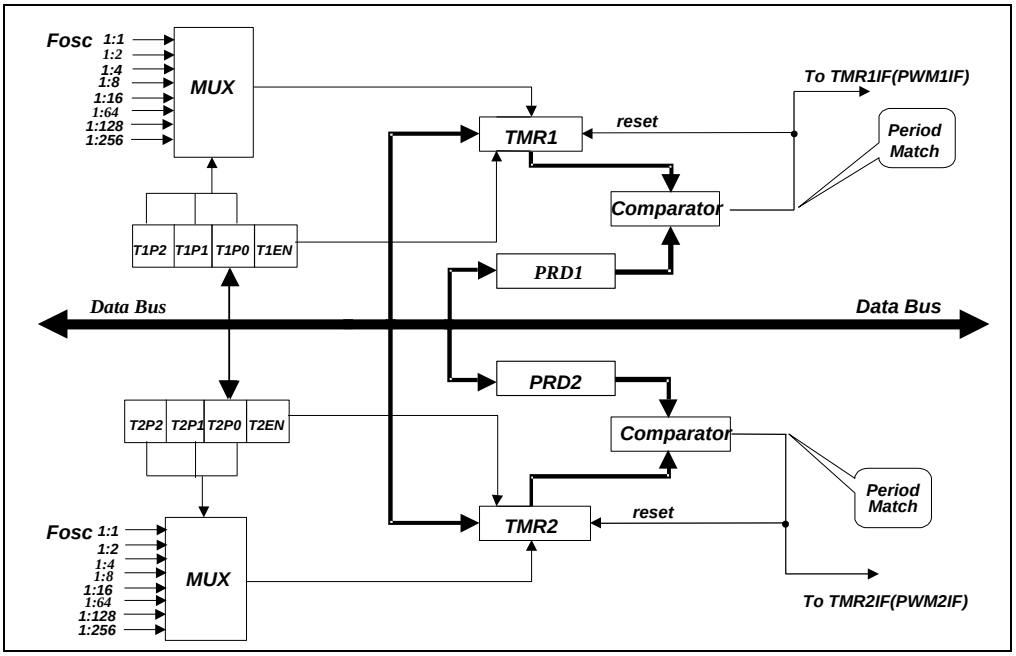


Figure 7-25 Timer Block Diagram

Where**:**

Fosc: Input clock.

Prescaler (T1P2, T1P1 and T1P0 / T2P2, T2P1 and T2P0): The options 1**:**1, 1**:**2, 1**:**4, 1**:**8, 1**:**16, 1**:**64, 1**:**128, and 1**:**256 are defined by TMRX. It is cleared when any type of reset occurs.

TMR1 and TMR2: Timer X register. TMRX is increased until it matches with PRDX, and then is reset to "**0**" (default value).

DT1 and DT2: Timer X register. TMRX is increased until it matches with DTX, and then is reset to "**0**" (default value).

PRDX (PRD1, PRD2): PWM time period register

Comparator X (Comparator 1 and Comparator 2): Reset TMRX while a match occurs. The TMRXIF (PWMXIF) flag is set at the same time.

7.9.3 Programming the Related Registers

When defining TMRX, refer to the operation of its related registers as shown in the following table. It must be noted that the PWMX bits must be disabled if their related TMRXs are utilized. That is, Bit 7 ~ Bit 3 of the PWMCON register must be set to "**0**".

■ Related Control Registers of TMR1 and TMR2

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x07	PWMCON/R7	IPWM2E	IPWM1E	"0"	"0"	"0"	PWMCAS	PWM2E	PWM1E
0x08	TMRCON/R8	T2EN	T1EN	T2P2	T2P1	T2P0	T1P2	T1P1	T1P0

7.9.4 Timer Programming Process/Steps

1. Load PRDX with the Timer duration
2. Enable interrupt function by writing IOCF0, if required
3. Load a desired value for the TMRX prescaler, enable TMRX and disable PWMX

7.9.5 PWM Cascade Mode

The PWM Cascade Mode merges two 8-bit PWM function into one 16-bit. In this mode, the necessary parameters are redefined as shown on the table below:

Parameter / 16-bit PWM	DT (Duty)	PRD (Period)	TMR (Timer)
MSB (15~8)	DT2	PRD2	TMR2
LSB (7~0)	DT1	PRD1	TMR1

The prescaler of this 16-bit PWM uses the prescaler of the TMR1. The MSB of TMR is counted when LSB carry and the PWM1IF bit/PWM1 pins are redefined as the PWMIF bit/PWM pin (or PWM1 pin).

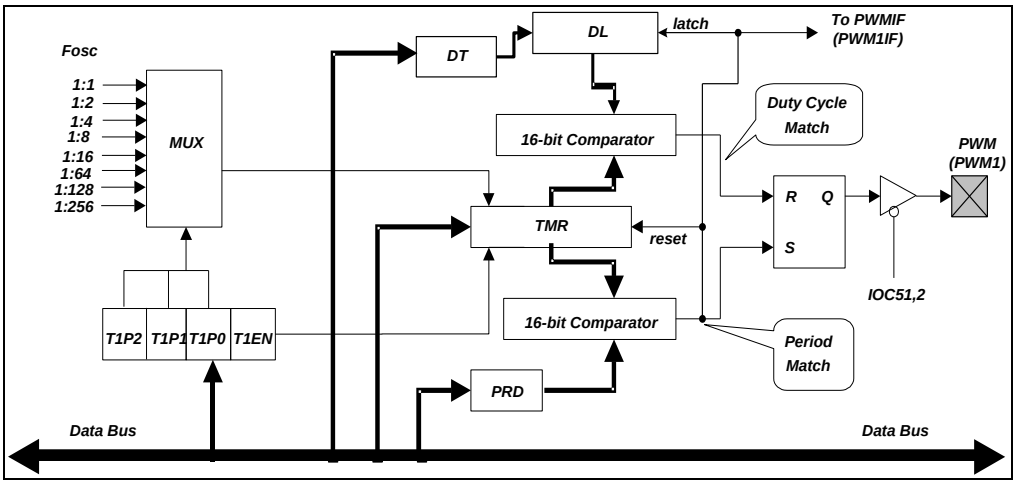


Figure 7-26 16-Bit PWM Functional Block Diagram (Merged from Two 8 Bits)

7.11 Oscillator

7.11.1 Oscillator Modes

The EM78P302N can be operated in seven different oscillator modes, such as Crystal Oscillator Mode (XT), High Crystal Oscillator Mode 1 (HXT1), High Crystal Oscillator Mode 2 (HXT2), Low Crystal Oscillator Mode 1 (LXT1), Low Crystal Oscillator Mode 2 (LXT2), RC Oscillator Mode with Internal RC Oscillator Mode (IRC). You can select one of them by programming the OSC3 ~ OSC0 in the Code Option register.

The Oscillator modes defined by OSC3 ~ OSC0 are described below.

Oscillator Modes	OSC3	OSC2	OSC1	OSC0
Reserved	0	0	0	0
Reserved	0	0	0	1
IRC[1] (Internal RC oscillator mode); P55/ADC6/OSCO acts as P55 P70/ADC5/OSCI/RCOUT acts a P70 (Default)	0	0	1	0
IRC[1] (Internal RC oscillator mode); P55/ADC6/OSCO acts as P55 P70/ADC5/OSCI/RCOUT acts as RCOUT	0	0	1	1
LXT1[2] (Frequency range of XT, mode is 100kHz ~ 1 MHz)	0	1	0	0
HXT1[2] (Frequency range of XT mode is 12 MHz ~ 20 MHz)	0	1	0	1
LXT2[2] (Frequency range of XT mode is 32.768kHz)	0	1	1	0
HXT2[2] (Frequency range of XT mode is 6 MHz ~ 12 MHz)	0	1	1	1
XT[2] (Frequency range of XT mode is 1 MHz ~ 6 MHz)	1	1	1	1

[1] *In IRC mode, P55 is normal I/O pin. RCOUT/P70 is defined by Code Option Word 1 Bit4 ~Bit 1.*

[2] *In LXT1, LXT2, HXT1, HXT2 and XT modes; OSCI and OSCO are used as oscillator pins. These pins cannot and should not be defined as normal I/O pins.*

The maximum operating frequency limit of crystal/resonator at different VDDs, are as follows**:**

Conditions	VDD	Max. Freq. (MHz)
Two clocks	2.1V	4
	3.0V	8
	4.5V	16

7.11.2 Crystal Oscillator/Ceramic Resonators (Crystal)

The EM78P302N can be driven by an external clock signal through the OSCI pin as illustrated below.

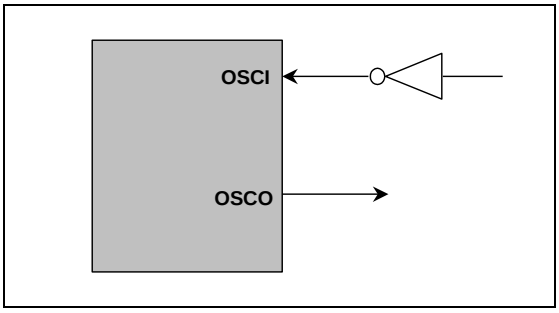


Figure 7-29 External Clock Input Circuit

In most applications, Pin OSCI and Pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation. Figure 7-31 below depicts such a circuit. The same applies to the XT mode, HXT1 mode, HTX2 mode, LXT1 mode and LXT2 mode.

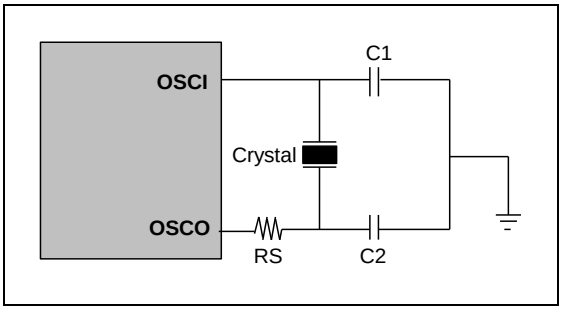


Figure 7-30 Crystal/Resonator Circuit

The following table provides the recommended values for C1 and C2. Since each resonator has its own attribute, user should refer to the resonator specifications for the appropriate values of C1 and C2. RS, a serial resistor, maybe required for AT strip cut crystal or low frequency mode. **When the system works in Crystal mode (16 MHz), a 10 KΩ is connected between OSCI and OSCO.**

Capacitor selection guide for crystal oscillator or ceramic resonators:

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
Ceramic Resonators	LXT1 (100 K ~ 1 MHz)	100kHz	60 pF	60 pF
		200kHz	60 pF	60 pF
		455kHz	40 pF	40 pF
		1 MHz	30 pF	30 pF
	XT (1 M ~ 6 MHz)	1.0 MHz	30 pF	30 pF
		2.0 MHz	30 pF	30 pF
		4.0 MHz	20 pF	20 pF
Crystal Oscillator	LXT2 (32.768kHz)	32.768kHz	40 pF	40 pF
	LXT1 (100 K ~ 1 MHz)	100kHz	60 pF	60 pF
		200kHz	60 pF	60 pF
		455kHz	40 pF	40 pF
		1 MHz	30 pF	30 pF
	XT (1~6 MHz)	1.0 MHz	30 pF	30 pF
		2.0 MHz	30 pF	30 pF
		4.0 MHz	20 pF	20 pF
		6.0 MHz	30 pF	30 pF
	HXT2 (6~12 MHz)	6.0 MHz	30 pF	30 pF
		8.0 MHz	20 pF	20 pF
		12.0 MHz	30 pF	30 pF
	HXT1 (12~20 MHz)	12.0 MHz	30 pF	30 pF
		16.0 MHz	20 pF	20 pF

Circuit diagrams for serial and parallel modes Crystal/Resonator:

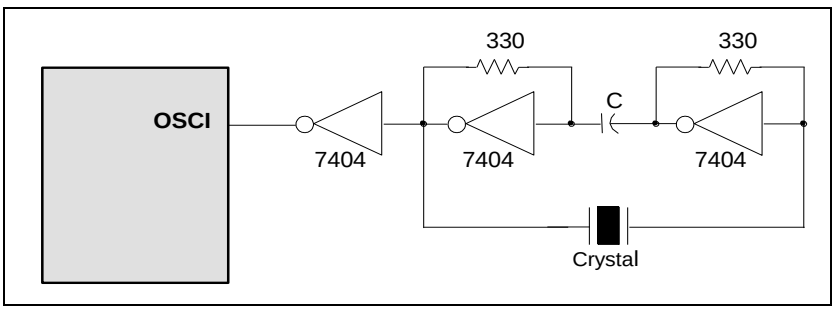


Figure 7-31 Serial Mode Crystal/Resonator Circuit Diagram

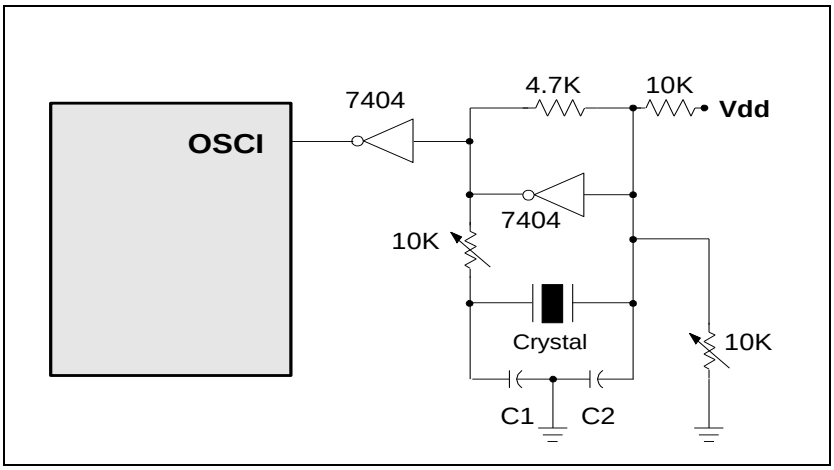


Figure 7-32 Parallel Mode Crystal/Resonator Circuit Diagram

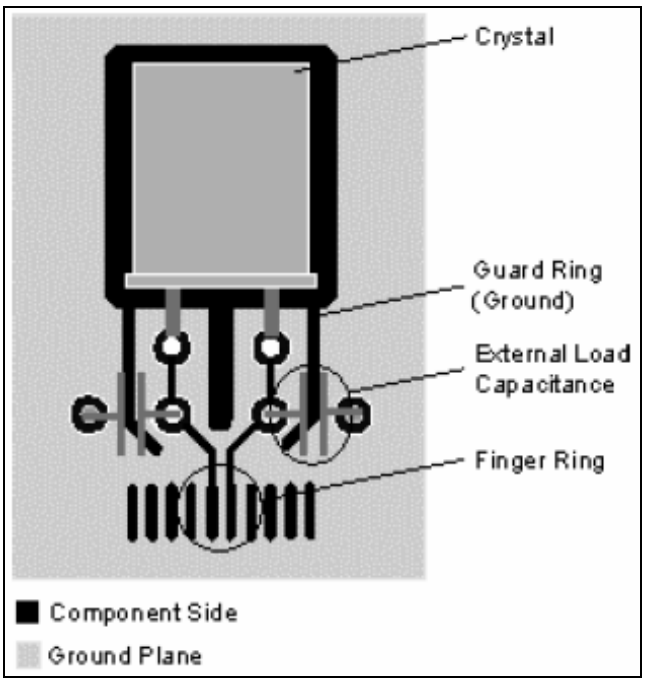


Figure 7-33 Parallel Mode Crystal/Resonator Circuit Diagram

7.11.4 Internal RC Oscillator Mode

The EM78P302N offers a versatile internal RC mode with default frequency value of 4 MHz. The Internal RC oscillator mode has other frequencies (16 MHz, 8 MHz, and 1 MHz) that can be set by Code Option (Word 1), RCM1, and RCM0. The Table below describes the EM78P302N internal RC drift with voltage, temperature, and process variations.

Internal RC Drift Rate (Ta=25°C, VDD=5V±5%, VSS=0V)

Internal RC Frequency	Drift Rate			
	Temperature (-40°C ~+85°C)	Voltage (2.1V~5.5V)	Process	Total
4 MHz	±2%	±1%	±1%	±4%
16 MHz	±2%	±1%	±1%	±4%
8 MHz	±2%	±1%	±1%	±4%
1 MHz	±2%	±1%	±1%	±4%

Note: *Theoretical values are for reference only. Actual values may vary depending on the actual process.*

7.12 Power-on Considerations

Any microcontroller is not warranted to start operating properly before the power supply stabilizes in steady state. The EM78P302N POR voltage range is 1.9V ± 0.2V. Under customer application, when power is switched OFF, Vdd must drop below 1.6V and remains at OFF state for 10μs before power can be switched ON again. Subsequently, the EM78P302N will reset and work normally. The extra external reset circuit will work well if Vdd rises fast enough (50ms or less). However, under critical applications, extra devices are still required to assist in solving power-on problems.

7.12.1 Programmable WDT Time-out Period

The Option word (WDTPS) is used to define the WDT time-out period (18ms[5] or 4.5ms[6]). Theoretically, the range is from 4.5ms or 18ms. For most crystal or ceramic resonators, the lower the operation frequency is, the longer is the required set-up time.

[5] VDD=5V, WDT time-out period = 16.5ms ± 30%.
VDD=3V, WDT time-out period = 18ms ± 30%.

[6] VDD=5V, WDT time-out period = 4.2ms ± 30%.
VDD=3V, WDT time-out period = 4.5ms ± 30%.

7.12.2 External Power-on Reset Circuit

The circuit shown in the following figure implements an external RC to produce a reset pulse. The pulse width (time constant) should be kept long enough to allow the Vdd to reach the minimum operating voltage. This circuit is used when the power supply has a slow power rise time. Because the current leakage from the /RESET pin is about ± 5μA, it is recommended that R should not be greater than 40KΩ. This way, the voltage at Pin /RESET is held below 0.2V. The diode (D) functions as a short circuit at power-down. The "C" capacitor is discharged rapidly and fully. Rin, the current-limited resistor, prevents high current discharge or ESD (electrostatic discharge) from flowing into Pin /RESET.

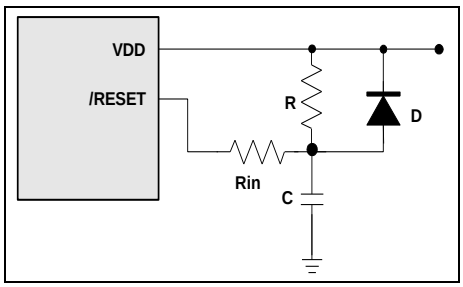


Figure 7-35 External Power-on Reset Circuit

7.12.3 Residual Voltage Protection

When the battery is replaced, device power (Vdd) is removed but residual voltage remains. The residual voltage may trip below Vdd minimum, but not to zero. This condition may cause a poor power-on reset. Figure 7-36 and Figure 7-37 show how to create a protection circuit against residual voltage.

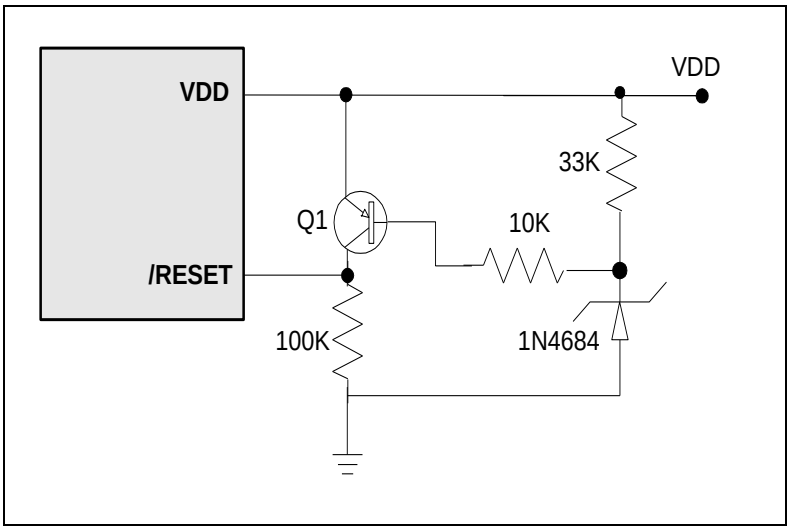


Figure 7-36 Residual Voltage Protection Circuit 1

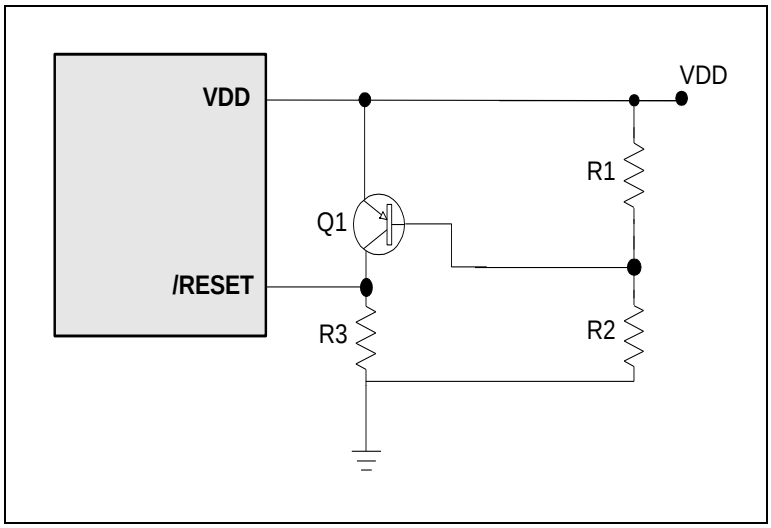


Figure 7-37 Residual Voltage Protection Circuit 2

7.13 Code Option

EM78P302N has four Code Option Words and two Customer ID words that are not part of the normal program memory.

Word 0	Word1	Word 2	Word 3	Word E	Word 0x10	Word 0x11
Bits 12~0	Bits 12~0	Bits12~0	Bits12~0	Bits12~0	Bits12~0	Bits12~0

7.13.1 Code Option Register (Word 0)

Word 0											
Bit	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bits 2~0**
Mnemonic	-	P70_HD/HS	WK_CLK	CLKS	LVR1	LVR0	RESETEN	ENWDT	NRHL	NRE	Protect
1	-	Disable	8 clock	High	High	High	Disable	Disable	32/fc	Enable	Disable
0	-	Enable	32 clock	Low	Low	Low	Enable	Enable	8/fc	Disable	Enable

Bit 12: Not used (Reserved). This bit is set to "1" all the time.

Bit 11 (P70_HD/HS) :

0 : Enable

1 : Disable (default)

Bit 10 (WK_CLK) : Selecting 8 or 32 clocks wake up from sleep and idle mode (only IRC mode)

0 : 32 clocks

1 : 8 clocks (default)

Bit 9 (CLKS): Instruction period option bit

0 = two oscillator periods

1 = four oscillator periods (default)

Bits 8~7 (LVR1 ~ LVR0): Low Voltage Reset Enable bits

LVR1, LVR0	VDD Reset Level	VDD Release Level
11	NA (Power-on Reset) (Default)	
10	2.7V	2.9V
01	3.5V	3.7V
00	4.0V	4.2V

Bit 6 (RESETEN): RESET/P71 Pin Select Bit

0 : P71 set to /RESET pin

1 : P71 is general purpose input pin or open-drain for output Port (default)

Bit 5 (ENWDT): Watchdog timer enable bit

0 = Enable

1 = Disable (default)

Bit 4 (NRHL): Noise rejection high/low pulses define bit. INT pin is falling or rising edge trigger

0 : Pulses equal to 8/fc is regarded as signal

1 : Pulses equal to 32/fc is regarded as signal (default)

NOTE

The noise rejection function is turned off in the LXT2 and sleep mode.

Bit 3 (NRE): Noise Rejection Enable

0 : Disable noise rejection

1 : Enable noise rejection (default), but in Low Crystal oscillator (LXT) mode, the noise rejection circuit is always disabled.

Bits 2 ~ 0 (Protect**):** Protect Bit

Protect Bits	Protect
0	Enable
1	Disable (default)

7.13.2 Code Option Register (Word 1)

Word 1													
Bit	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	-	-	-	-	-	-	RCM1	RCM0	OSC3	OSC2	OSC1	OSC0	RCOUT
1	-	-	-	-	-	-	High	High	High	High	High	High	System_clk
0	-	-	-	-	-	-	Low	Low	Low	Low	Low	Low	Open_drain

Bits 12~7 (C5~C0): Not used (reserved). This bit is set to "1" all the time

Bits 6~5 (RCM1, RCM0): RC mode select bits

RCM 1	RCM 0	Frequency (MHz)
1	1	4 (Default)
1	0	16
0	1	8
0	0	1

Bits 4 ~ 1 (OSC3 ~ OSC0): Oscillator Modes Select bits

Oscillator Modes	OSC3	OSC2	OSC1	OSC0
Reserved	0	0	0	0
Reserved	0	0	0	1
IRC[1] (Internal RC oscillator mode); P55/ADC6/OSCO acts as P55 P70/ADC5/OSCI/RCOUT acts as P70 (default)	0	0	1	0
IRC[1] (Internal RC oscillator mode); P55/ADC6/OSCO acts as P55 P70/ADC5/OSCI/RCOUT acts as RCOUT	0	0	1	1
LXT1[2] (Frequency range of XT, mode is 100kHz~1MHz)	0	1	0	0
HXT1[2] (Frequency range of XT mode is 12MHz~20MHz)	0	1	0	1
LXT2[2] (Frequency range of XT mode is 32.768kHz)	0	1	1	0
HXT2[2] (Frequency range of XT mode is 6MHz~12MHz)	0	1	1	1
XT[2] (Frequency range of XT mode is 1MHz~6MHz)	1	1	1	1

[1] *In IRC mode, P55 is normal I/O pin. RCOUT/P70 is defined by Code Option Word 1 Bit4 ~Bit 1.*

[2] *In LXT1, LXT2, HXT1, HXT2 and XT modes; OSCI and OSCO are used as oscillator pins. These pins cannot and should not be defined as normal I/O pins.*

Bit 0 (RCOUT): Instruction clock output enable bit in IRC mode.

0 : RCOUT pin output instruction clock with open drain.

1 : RCOUT pin output instruction clock(default)

7.13.3 Code Option Register (Word 2)

Word 2													
Bit	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	–	–	–	SFS	–	IRCPSS	–	HLP	–	WDTPS	RLEN	SHEN	SHSEL
1	–	–	–	16KHz	–	Internal	–	High	–	18ms	No Reload	Enable	8 clks
0	–	–	–	128KHz	–	VDD	–	Low	–	4.5ms	Reload	Disable	0.5 clks

Bit 12: Not used, (reserved). This bit is set to “1” all the time.

Bit 11: Not used, (reserved). This bit is set to “0” all the time.

Bit 10: Not used, (reserved). This bit is set to “1” all the time.

Bit 9 (SFS): Sub-oscillator select for GREEN mode and TCC, PWM1, PWM2 clock source.
(Not include WDT time-out and free run setup-up time)

0 : 128kHz

1 : 16kHz (default)

Bit 8: Not used, (reserved). This bit is set to “0” all the time.

Bit 7 (IRCPSS): IRC Power Source Select

0 = VDD

1 = Internal reference (default)

Bit 6: Not used (reserved). This bit is set to “0” all the time.

Bit 5 (HLP): **Power consumption selection**

0: Low power consumption mode, applies to operating frequency at 400 kHz or below 400kHz

1: High power consumption mode, applies to operating frequency above 400 kHz (Default)

(User selects LXT1 or LXT2 in crystal mode, HLP function automatically selects low)

Bit 4 (LPS): Not used, (reserved). This bit is set to “1” all the time.

Bit 3 (WDTPS): WDT Time-out Period

WDT Time	Watchdog Timer*
1	18 ms (Default)
0	4.5 ms

*Theoretical values, for reference only.

Bit 2 (RLEN): Reload Enable

0: Program code reloaded

1: No reload function

Bit 1 (SHEN): System Hold Enable

0: Disable

1: Enable

Bit 0 (SHSEL): System Hold clock selection

0: 0.5 clock delay when system hold activated

1: 8 clock delay when system hold activated

7.13.4 Code Option Register (Word 3)

Word 3													
Bit	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	ID12	ID11	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID13	ID2	ID1	ID0
1	High	High	High	High	High	High	High	High	High	High	High	High	High
0	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low

Bits 12 ~ 0: Customer's ID code

7.13.4 Code Option Register (Word E)

Word 3													
Bit	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	-	-	ADPIN OPT	/REFSEL	-	CT3	CT2	CT1	CT0	RT3	RT2	RT1	RT0
1	-	-	High	High	-	High	High	High	High	High	High	High	High
0	-	-	Low	Low	-	Low	Low	Low	Low	Low	Low	Low	Low

Bits 12 ~ 11: Not used, (reserved).

Bit 10 (ADPINOPT): ADC4 pin location select bit.

0: The ADC4 at P54/TCC/ADC4/VREF.

1: The ADC4 at P67/ADC4/PWM1.

Bit 9 (VREFSEL): ADC internal reference voltage select. [Depend on VREF[1:0] (Bank 0-RA[2:1]) = 11]

0: ADC Internal reference voltage 2.5V.

1: ADC Internal reference voltage 2.0V. (Default)

Bit 8: Not used (reserved)

Bits 7 ~ 4 (CT3 ~ CT0): Internal RC mode Capacitance Trim bits (Coarse Calibration). These bits must always be set to “1” only (auto calibration).

Trimming Code				CLK Period	Frequency
CT[3]	CT[2]	CT[1]	CT[0]		
0	0	0	0	Period*(1+40%)	F*(1-28.57%)
0	0	0	1	Period*(1+35%)	F*(1-25.93%)
0	0	1	0	Period*(1+30%)	F*(1-23.08%)
0	0	1	1	Period*(1+25%)	F*(1-20.00%)
0	1	0	0	Period*(1+20%)	F*(1-16.67%)
0	1	0	1	Period*(1+15%)	F*(1-13.04%)
0	1	1	0	Period*(1+10%)	F*(1-9.09%)
0	1	1	1	Period*(1+5%)	F*(1-4.76%)
1	1	1	1	Period (default)	F (default)
1	1	1	0	Period*(1-5%)	F*(1+5.26%)
1	1	0	1	Period*(1-10%)	F*(1+11.11%)
1	1	0	0	Period*(1-15%)	F*(1+17.65%)
1	0	1	1	Period*(1-20%)	F*(1+25.00%)
1	0	1	0	Period*(1-25%)	F*(1+33.33%)
1	0	0	1	Period*(1-30%)	F*(1+42.86%)
1	0	0	0	Period*(1-35%)	F*(1+53.85%)

Bits 3 ~ 0 (RT3 ~ RT0): Internal RC mode Resistance Trim bits (Fine Calibration).
These bits must always be set to “1” only (auto calibration).

Trimming Code				CLK Period	Frequency
RT[3]	RT[2]	RT[1]	RT[0]		
0	0	0	0	Period*(1+8%)	F*(1-7.41%)
0	0	0	1	Period*(1+7%)	F*(1-6.54%)
0	0	1	0	Period*(1+6%)	F*(1-5.66%)
0	0	1	1	Period*(1+5%)	F*(1-4.76%)
0	1	0	0	Period*(1+4%)	F*(1-3.85%)
0	1	0	1	Period*(1+3%)	F*(1-2.91%)
0	1	1	0	Period*(1+2%)	F*(1-1.96%)
0	1	1	1	Period*(1+1%)	F*(1-0.99%)
1	1	1	1	Period (default)	F (default)
1	1	1	0	Period*(1-1%)	F*(1+1.01%)
1	1	0	1	Period*(1-2%)	F*(1+2.04%)
1	1	0	0	Period*(1-3%)	F*(1+3.09%)
1	0	1	1	Period*(1-4%)	F*(1+4.17%)
1	0	1	0	Period*(1-5%)	F*(1+5.26%)
1	0	0	1	Period*(1-6%)	F*(1+6.38%)
1	0	0	0	Period*(1-7%)	F*(1+7.53%)

7.13.5 Customer ID Register (Word 0x10)

Word 0x10													
Bit	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	ID25	ID24	ID23	ID22	ID21	ID20	ID19	ID18	ID17	ID16	ID15	ID14	ID13
1	High	High	High	High	High	High	High	High	High	High	High	High	High
0	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low

Bits 12 ~ 0: Customer's ID Ⅱ code (Can be read from Table Point Register)

7.13.6 Customer ID Register (Word 0x11)

Word 0x11													
Bit	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	ID38	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	ID29	ID28	ID27	ID26
1	High	High	High	High	High	High	High	High	High	High	High	High	High
0	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low

Bits 12 ~ 0: Customer's ID Ⅲ code (Can be read from Table Point Register)

7.14 Low Voltage Reset

The low voltage reset (LVR) is designed for unstable power situation, such as external power noise interference or in EMS test condition.

When LVR is enabled, the system supply voltage (V_{DD}) drops below V_{DD} reset level (V_{RESET}) and remains at 10μs, a system reset will occur and the system will remain in reset status. The system will remain at reset status until V_{DD} voltage rise above V_{DD} release level.

7.14.1 Low Voltage Reset

LVR property is set at Bits 8 and 7 of Code Option Word 0. Detailed operation mode is as follows:

Word 0										
Bit 12	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bits 2~0**
-	P70_HD/HS	WK_CLK	CLKS	LVR1	LVR0	RESETEN	ENWDT	NRHL	NRE	Protect

Bits 8~7 (LVR1 ~ LVR0): Low Voltage Reset Enable bits

LVR1, LVR0	VDD Reset Level	VDD Release Level
11	NA (Power-on Reset)	
10	2.7V	2.9V
01	3.5V	3.7V
00	4.0V	4.2V

7.15 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of two oscillator time periods), unless the program counter is changed by instructions "MOV R2,A, "ADD R2,A," or by instructions of arithmetic or logic operation on R2 (e.g., "SUB R2,A," "BS(C) R2,6," "CLR R2," etc.).

In addition, the instruction set has the following features:

1. Every bit of any register can be set, cleared, or tested directly.
2. The I/O registers can be regarded as general registers. That is, the same instruction can operate on I/O registers.

The following symbols are used in the Instruction Set table:

Convention:

R *= Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.*

Bits 6 and 7 in R4 determine the selected register bank.

b *= Bit field designator that selects the value for the bit located in the register R and which affects the operation.*

k *= 8 or 10-bit constant or literal value*

Mnemonic	Operation	Status Affected
NOP	No Operation	None
DAA	Decimal Adjust A	C
CONTW	A → CONT	None
SLEP	0 → WDT, Stop oscillator	T, P
WDTC	0 → WDT	T, P
IOW R	A → IOCR	None[1]
ENI	Enable Interrupt	None
DISI	Disable Interrupt	None
RET	[Top of Stack] → PC	None
RETI	[Top of Stack] → PC, Enable Interrupt	None
CONTR	CONT → A	None
IOR R	IOCR → A	None[1]
MOV R,A	A → R	None
CLRA	0 → A	Z
CLR R	0 → R	Z
SUB A,R	R-A → A	Z, C, DC
SUB R,A	R-A → R	Z, C, DC
DECA R	R-1 → A	Z
DEC R	R-1 → R	Z
OR A,R	A ∨ VR → A	Z
OR R,A	A ∨ VR → R	Z
AND A,R	A & R → A	Z
AND R,A	A & R → R	Z

Mnemonic	Operation	Status Affected
XOR A,R	A ⊕ R → A	Z
XOR R,A	A ⊕ R → R	Z
ADD A,R	A + R → A	Z, C, DC
ADD R,A	A + R → R	Z, C, DC
MOV A,R	R → A	Z
MOV R,R	R → R	Z
COMA R	/R → A	Z
COM R	/R → R	Z
INCA R	R+1 → A	Z
INC R	R+1 → R	Z
DJZA R	R-1 → A, skip if zero	None
DJZ R	R-1 → R, skip if zero	None
RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
SWAP R	R(0-3) ↔ R(4-7)	None
JZA R	R+1 → A, skip if zero	None
JZ R	R+1 → R, skip if zero	None
BC R,b	0 → R(b)	None [2]
BS R,b	1 → R(b)	None [3]
JBC R,b	if R(b)=0, skip	None
JBS R,b	if R(b)=1, skip	None
CALL k	PC+1 → [SP], (Page, k) → PC	None
JMP k	(Page, k) → PC	None
MOV A,k	k → A	None
OR A,k	A ∨ k → A	Z
AND A,k	A & k → A	Z
XOR A,k	A ⊕ k → A	Z
RETL k	k → A, [Top of Stack] → PC	None
SUB A,k	k-A → A	Z, C, DC
Add A,K	k+A → A	Z, C, DC
BANK k	k → R4(6)	None
LCALL k	PC+1→[SP], k→PC	None
LJMP k	k→PC	None
TBRD R	If Bank1 R5.7=0, machine code (7~0) → R Else Bank1 R5.7=1, machine code (12~8) → R(4~0), R(7~5)=(0,0,0)	None

Note: *1 This instruction is applicable to IOC50~IOCF0, IOC51 ~ IOCF1 only.*
2 This instruction is not recommended for RF operation.
3 This instruction cannot operate under RF.

8 Absolute Maximum Ratings

Items	Rating		
Temperature under bias	-40°C	to	85°C
Storage temperature	-65°C	to	150°C
Input voltage	Vss-0.3V	to	Vdd+0.5V
Output voltage	Vss-0.3V	to	Vdd+0.5V
Working Voltage	2.1V	to	5.5V
Working Frequency	DC	to	16 MHz

9 DC Electrical Characteristics

Ta= 25°C, VDD= 5.0V, VSS= 0V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
FXT	Crystal: VDD to 5V	Two cycles with two clocks	32.768k	4	16	MHz
VIH1	Input High Voltage (Schmitt Trigger)	Ports 5, 6, 7	0.7VDD	–	VDD+0.3	V
VIL1	Input Low Voltage (Schmitt Trigger)	Ports 5, 6, 7	-0.3V	–	0.3VDD	V
VIHT1	Input High Threshold Voltage (Schmitt Trigger)	/RESET	–	1.8	–	V
VILT1	Input Low Threshold Voltage (Schmitt Trigger)	/RESET	–	1.1	–	V
VIHT2	Input High Threshold Voltage (Schmitt Trigger)	TCC, INT	0.7VDD	–	VDD+0.3	V
VILT2	Input Low Threshold Voltage (Schmitt Trigger)	TCC, INT	-0.3V	–	0.3VDD	V
IOH1	Output High Voltage (Ports 5, 6, 7)	VOH = 0.9VDD	–	-8	–	mA
IOH2	Output High Voltage (Ports 51~54, 56~57,60, 67)		–	-18	–	
IOL1	Output Low Voltage (Ports 5, 6, 7)	VOL = 0.1VDD	–	15	–	mA
IOL2	Output Low Voltage (Ports 51~54, 56~57, 60, 67)		–	25	–	

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
LVR1	Low voltage reset level	Ta=25°C	2.41	2.7	2.99	V
		Ta=-40~85°C	2.14	2.7	3.25	V
LVR2	Low voltage reset level	Ta=25°C	3.1	3.5	3.92	V
		Ta=-40~85°C	2.73	3.5	4.25	V
LVR3	Low voltage reset level	Ta=25°C	3.56	4.0	4.43	V
		Ta=-40~85°C	3.16	4.0	4.81	V
IPH	Pull-high current	Pull-high active, input pin at VSS	–	70	–	μA
IPL	Pull-low current	Pull-low active, input pin at Vdd	–	40	–	μA
ISB1	Power down current	All input and I/O pins at VDD, output pin floating, WDT disabled	–	1.0	2.0	μA
ISB2	Power down current	All input and I/O pins at VDD, output pin floating, WDT enabled	–	–	10	μA
ICC1	Operating supply current at two clocks	/RESET= 'High', Fosc=32kHz (Crystal type, CLKS="0"), Output pin floating, WDT disabled	–	15	20	μA
ICC2	Operating supply current at two clocks	/RESET= 'High', Fosc=32kHz (Crystal type,CLKS="0"), output pin floating, WDT enabled	–	15	25	μA
ICC3	Operating supply current at two clocks	/RESET= 'High', Fosc=4 MHz (Crystal type, CLKS="0"), output pin floating, WDT enabled	–	1.5	1.7	mA
ICC4	Operating supply current at two clocks	/RESET= 'High', Fosc=10 MHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled	–	2.8	3.0	mA

***Note**: 1. These parameters are hypothetical (not tested) and are provided for design reference use only.*

2. Data under Minimum, Typical, and Maximum (Min, Typ, and Max) columns are based on hypothetical results at 25°C. These data are for design reference only.

9.1 AD Converter Characteristics

Vdd=2.5V to 5.5V, Vss=0V, Ta=-40 to 85°C

Symbol		Parameter	Condition	Min.	Typ.	Max.	Unit
V_{AREF}		Analog reference voltage	V_{AREF} - V_{ASS} ≥ 2.5V	2.5	–	Vdd	V
V_{ASS}				Vss	–	Vss	V
VAI		Analog input voltage	–	V_{ASS}	–	V_{AREF}	V
IAI1	Ivdd	Analog supply current	VAREF=VDD=5.0V, VASS=0.0V (VREF is internal VDD)	–	–	1400	µA
	Ivref			–	–	10	µA
IAI2	Ivdd	Analog supply current	VAREF=VDD=5.0V, VASS=0.0V (VREF is external VREF pin)	–	–	900	µA
	IVref			–	–	500	µA
RN		Resolution	–	–	12	–	Bits
INL		Integral Nonlinearity	VAREF=VDD=EXTERNAL_VREF=5.0V VASS=0.0V	–	–	±6	LSB
			VAREF=INTERNAL_VREF =2.0V/2.5V/3.0V/4.0V VASS=0.0V	–	–	±12	
DNL		Differential nonlinear error	VAREF=VDD=5.0V VASS=0.0V	–	–	±1	LSB
FSE		Full scale error	VAREF=VDD=5.0V VASS=0.0V	–	–	±8	LSB
OE		Offset error	VAREF= Vdd=5.0V VASS=0.0V	–	–	±4	LSB
ZAI		Recommended impedance of analog voltage source	–	–	–	10	KΩ
TAD		Period of ADC clock	VDD=3~5.5V, VASS = 0.0V,	1	–	–	µs
			VDD=2.5~3V, VASS = 0.0V,	2	–	–	µs

(Continuation)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tsh	Sample and Hold Time	VDD=3~5.5V, VASS = 0.0V, Ta=25°C	8	–	–	µs
		VDD=2.5~3V, VASS = 0.0V, Ta=25°C	16	–	–	µs
TCN	AD conversion time (Include S/H Time)	VDD=2.5~5.5V, VASS = 0.0V	14	–	24	TAD
TADD1	AD delay time between setting “ADRUN” and starting 1st TAD	VDD=2.5~5.5V, VASS=0.0V	0.5	–	–	TAD
PSR	Power Supply Rejection	VAREF= 2.5V, VAREF=2.5V, VASS=0V	–	–	2	LSB
$V_{1/4VDD}$	Accuracy for 1/4 VDD	–	–	±3	–	%
$V_{1/2VDD}$	Accuracy for 1/2 VDD	–	–	±3	–	%

Note:

1. *The parameters are theoretical values and have not been tested. Such parameters are for design reference only.*
2. *There is no current consumption when ADC is off other than minor leakage current.*
3. *AD conversion result will not decrease when an increase of input voltage and no missing code.*
4. *These parameters are subject to change without further notice.*

9.4 Vref 2V/2.5V/3V/4V Characteristics

Vdd = 5.0V, Vss=0V, Ta=-40 to 85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Power Supply	–	2.1	–	5.5	V
I_{VDD}	DC Supply Current	No load	–	–	250	µA
Vref	Voltage reference output	2V, 2.5V, 3V, 4V	–	±1	±1.75	%
Warn up time	Time ready for voltage reference	VDD = VDD_{min} - 5.5V, Cload = 19.2pf, Rload = 15.36KΩ	–	30	50	µs
VDD_{min}	Minimum Power Supply	–	–	Vref + 0.2*	–	V

*****VDD_{min} *: can work at (Vref+0.1V), but has a poor PSRR.*

10 AC Electrical Characteristics

Ta=-40 to 85°C, VDD=5V ± 5%, VSS=0V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type	125	–	DC	ns
Tpor	Delay Time after Power-On-Reset release	FSS0=1 (16kHz)	–	16 ± 30%	–	ms
Trstrl	Delay time after /Reset, WDT, and LVR release	Crystal type	–	WSTO + 510/Fm	–	μs
			–	WSTO + 8/Fs	–	μs
		IRC type	–	WSTO + 8/Fm	–	μs
			–	WSTO + 8/Fs	–	μs
Trsth1	Hold Time after /RESET pin reset	–	–	1 μs	–	–
Trsth2	Hold Time after LVR pin reset	–	–	1 μs	–	–
Twdt	Watchdog timer time-out	FSS0=1 (16kHz)	–	16 ± 30%	–	ms
Tset	Input pin setup time	–	–	0	–	ns
Thold	Input pin hold time	–	15	20	25	ns
Tdelay	Output pin delay time	Cload=20 pF Rload=1MΩ	–	20	–	ns

Note: 1. *WSTO: The waiting time of Start-to-Oscillation*

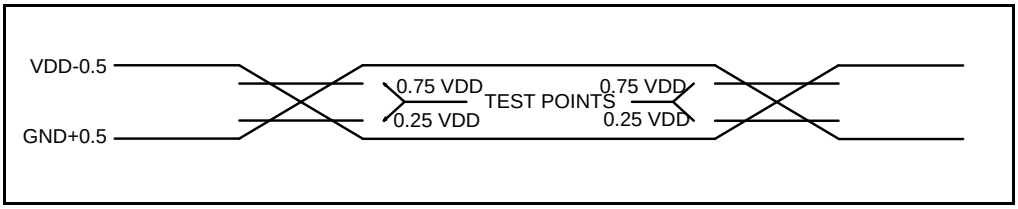
2. *These parameters are hypothetical (not tested) and are provided for design reference only.*

3. *Data under minimum, typical, and maximum (Min., Typ. and Max.) columns are based on hypothetical results at 25°C. These data are for design reference use only.*

****. Tpor*** *and* ***Twdt*** *are* ***16± 30%*** *ms at* ***FSS0=1(16kHz)****, Ta=-40°~85°C, and VDD=2.1~5.5V*

11 Timing Diagrams

AC Test Input / Output Waveform



Note: *AC Testing: Input are driven at VDD-0.5V for Logic "**1**" and GND+0.5V for Logic "**0**"*
*Timing measurements are made at 0.75V VDD for Logic "**1**" and 0.25V VDD for Logic "**0**"*

Figure 11-1a AC Test Input / Output Waveform Timing Diagram

Reset Timing (CLK="0")

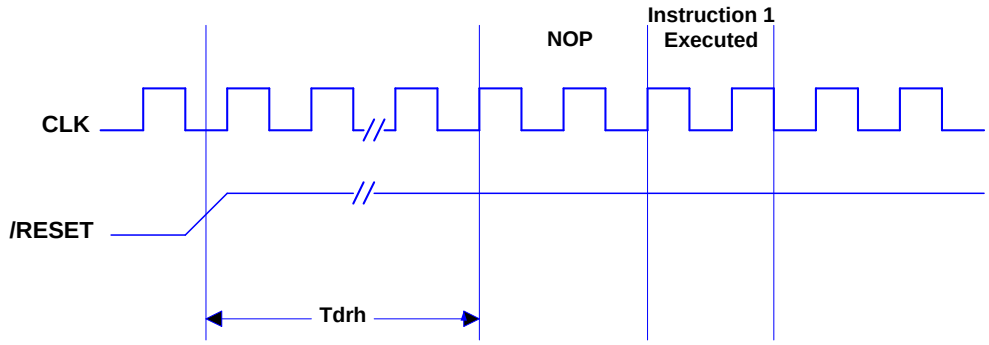


Figure 11-1b Reset Timing Diagram

TCC Input Timing (CLKS="0")

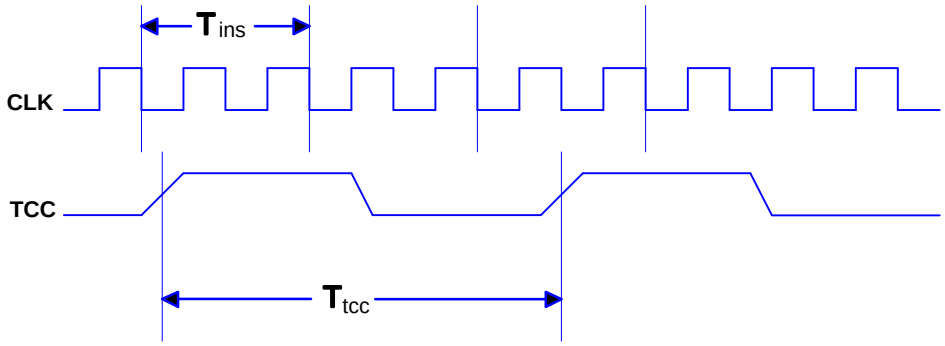
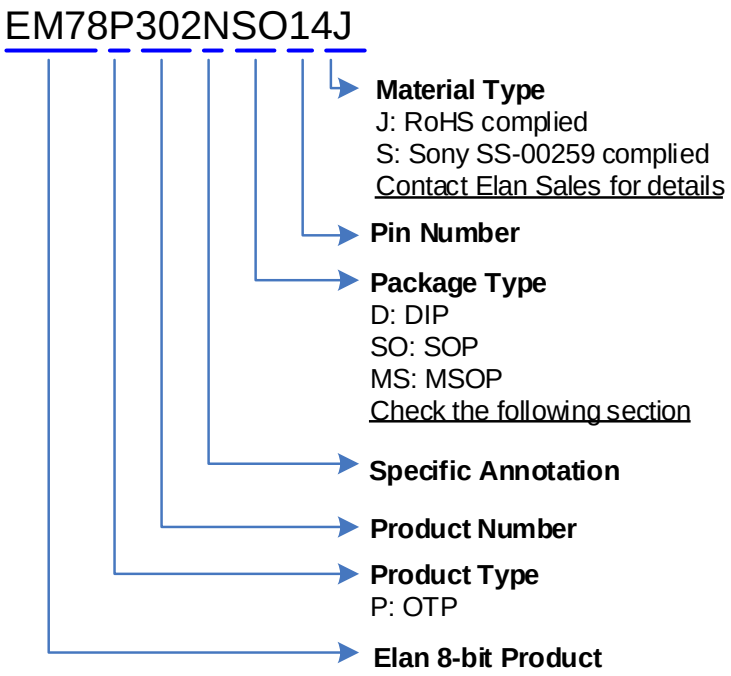


Figure 11-1c TCC Input Timing Diagram

APPENDIX

A Ordering and Manufacturing Information

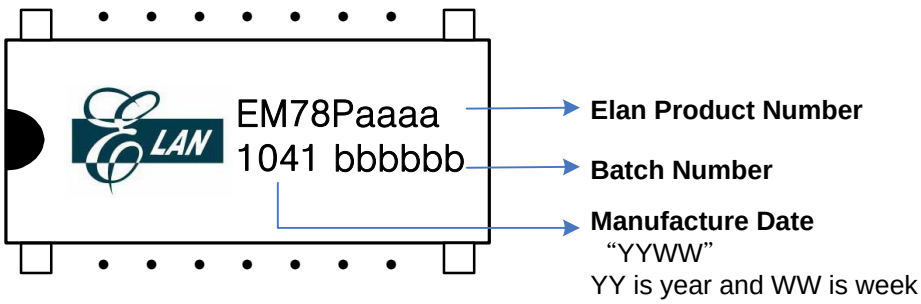


For example:

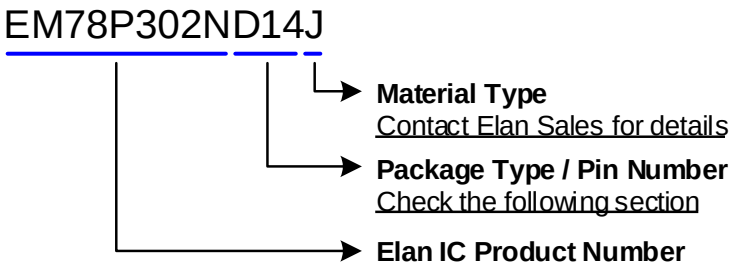
EM78P302ND14J

is EM78P302N with OTP program memory product, in 14-pin DIP 300mil package with RoHS complied

IC Mark



Ordering Code



B Package Type

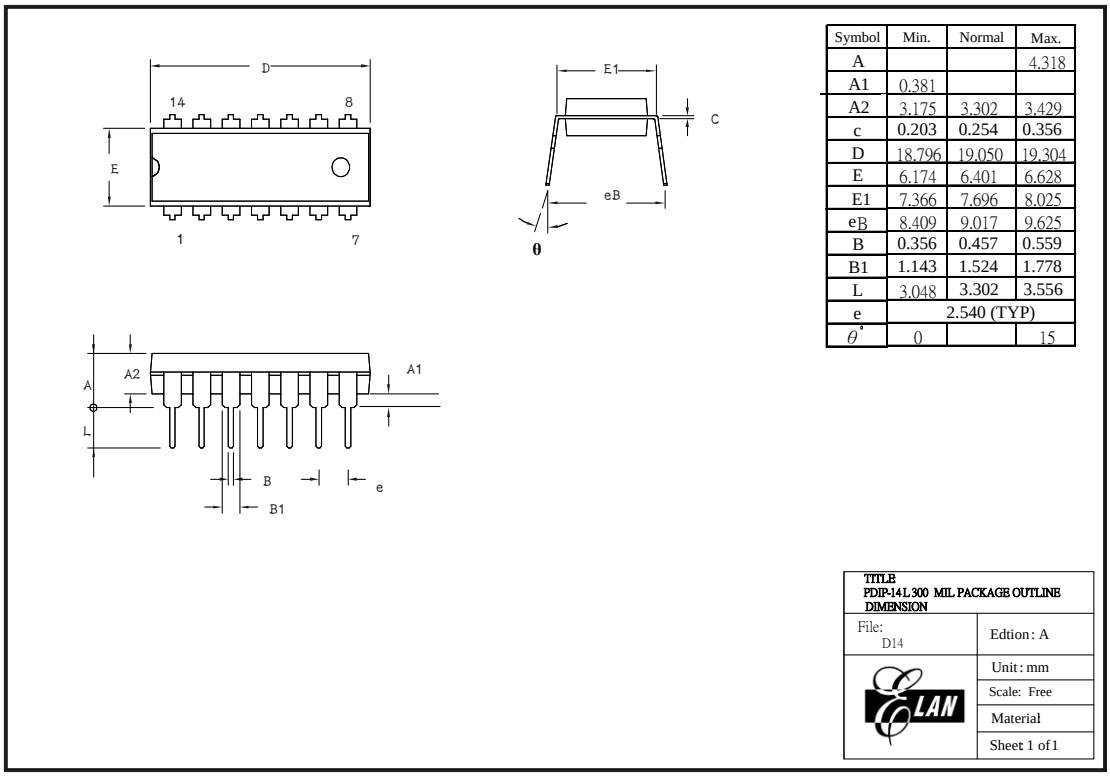
OTP MCU	Package Type	Pin Count	Package Size
EM78P302NMS10	MSOP	10	118 mil
EM78P302ND14	DIP	14	300 mil
EM78P302NSO14	SOP	14	150 mil

These are Green products and comply with RoHS specifications.

Part No.	EM78P302NxJ
Electroplate type	Pure Tin
Ingredient (%)	Sn: 100%
Melting point (°C)	232°C
Electrical resistivity (μΩ-cm)	11.4
Hardness (hv)	8~10
Elongation (%)	>50%

C Packaging Configuration

C.1 EM78P302ND14

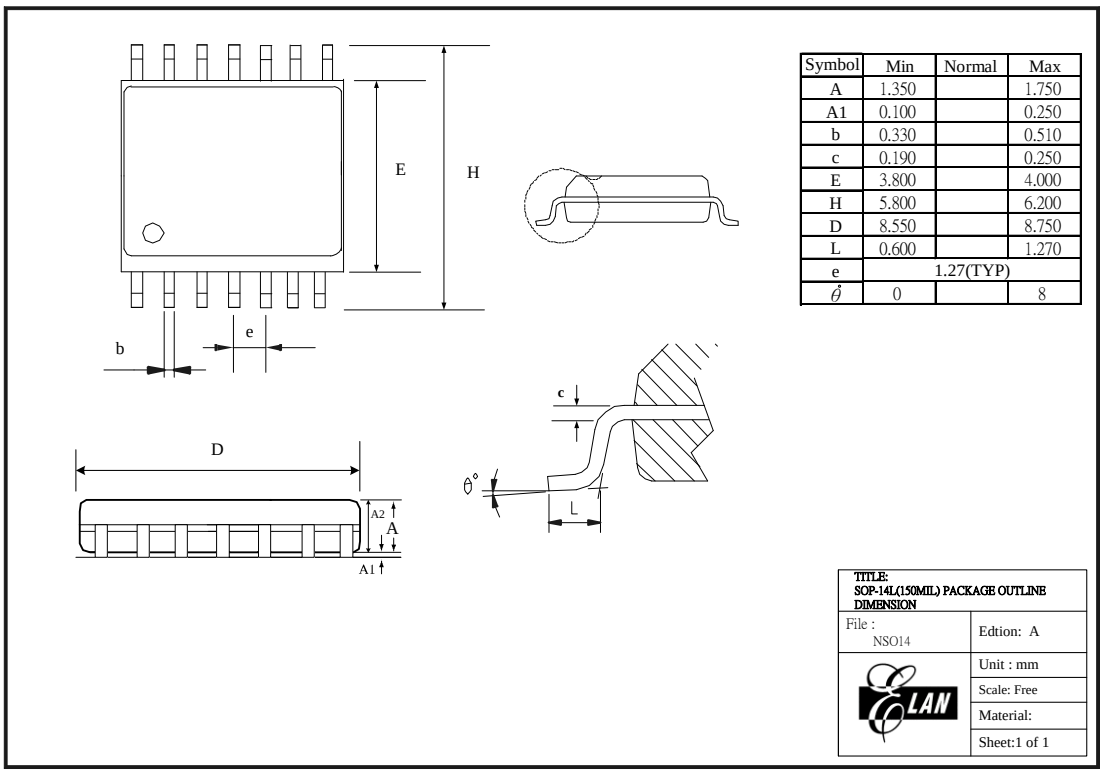


Symbol	Min.	Normal	Max.
A			4.318
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	18.796	19.050	19.304
E	6.174	6.401	6.628
E1	7.366	7.696	8.025
eB	8.409	9.017	9.625
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540 (TYP)		
θ°	0		15

TITLE: PDIP-14 L 300 MIL PACKAGE OUTLINE DIMENSION	
File: D14	Edtion: A
	Unit: mm
	Scale: Free
	Material
	Sheet 1 of 1

Figure C-1 EM78P302N 14-pin PDIP Package Type

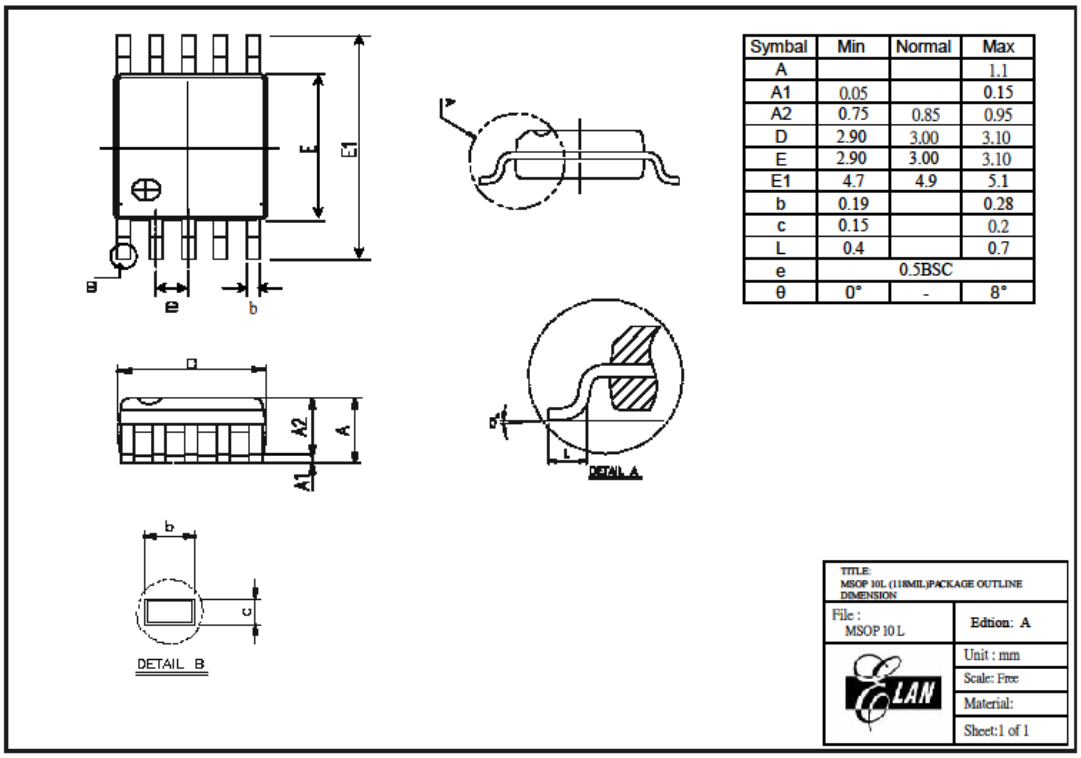
C.2 EM78P302NSO14



Symbol	Min	Normal	Max
A	1.350		1.750
A1	0.100		0.250
b	0.330		0.510
c	0.190		0.250
E	3.800		4.000
H	5.800		6.200
D	8.550		8.750
L	0.600		1.270
e	1.27(TYP)		
θ	0		8

Figure C-2 EM78P302N 14-pin SOP Package Type

C.3 EM78P302NMS10



Symbal	Min	Normal	Max
A			1.1
A1	0.05		0.15
A2	0.75	0.85	0.95
D	2.90	3.00	3.10
E	2.90	3.00	3.10
E1	4.7	4.9	5.1
b	0.19		0.28
c	0.15		0.2
L	0.4		0.7
e	0.5BSC		
θ	0°	-	8°

Figure C-3 EM78P302N 10-pin MSOP Package Type

D Quality Assurance and Reliability

Test Category	Test Conditions	Remarks
Solderability	Solder temperature=245 ± 5°C, for 5 seconds up to the stopper using a rosin-type flux	–
Pre-condition	Step 1: TCT, 65°C (15 min.)~150°C (15 min.), 10 cycles	For SMD IC (such as SOP, QFP, SOJ, etc)
	Step 2: Bake at 125°C, TD (durance) = 24 hrs	
	Step 3: Soak at 30°C /60% , TD (durance) = 192 hrs	
	Step 4: IR flow 3 cycles (Pkg thickness ≥ 2. 5 mm or Pkg volume ≥ 350 mm^3 – 225 ± 5°C) (Pkg thickness ≤ 2.5 mm or Pkg volume ≤ 350 mm^3 – 240 ± 5°C)	
Temperature cycle test	-65° (15 min.)~150°C (15 min.), 200 cycles	–
Pressure cooker test	TA = 121°C, RH = 100%, pressure = 2 atm, TD (durance) = 96 hrs	–
High temperature / High humidity test	TA=85°C , RH = 85% , TD (durance) = 168 , 500 hrs	–
High-temperature storage life	TA=150°C, TD (durance) = 500, 1000 hrs	–
High-temperature operating life	TA=125°C, VCC = Max. operating voltage, TD (durance) = 168, 500, 1000 hrs	–
Latch-up	TA=25°C, VCC = Max. operating voltage, 600mA/40V	–
ESD (HBM)	TA=25°C, ≥ | ± 4KV |	IP_ND,OP_ND,IO_ND IP_NS,OP_NS,IO_NS IP_PD,OP_PD,IO_PD, IP_PS,OP_PS,IO_PS, VDD-VSS(+),VDD_VSS (-) mode
ESD (MM)	TA=25°C, ≥ | ± 400V |	

D.1 Address Trap Detect

An address trap detect is one of the MCU embedded fail-safe functions that detects MCU malfunction caused by noise or the like. Whenever the MCU attempts to fetch an instruction from a certain section of ROM, an internal recovery circuit is auto started. If a noise-caused address error is detected, the MCU will repeat execution of the program until the noise is eliminated. The MCU will then continue to execute the next program.